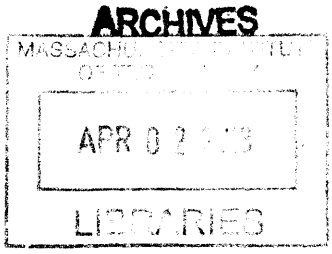
# Lossless Multi-Way Power Combining and Outphasing for Radio Frequency Power Amplifiers




by

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Submitted to the Department of Electrical Engineering and Computer Science
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## Abstract

For applications requiring the use of power amplifiers (PAs) operating at high frequencies and power levels, it is often preferable to construct multiple low power PAs and combine their output powers to form a high-power PA. Moreover, such PAs must often be able to provide dynamic control of their output power over a wide range, and maintain high efficiency across their operating range. This research work describes a new power combining and outphasing system that provides both high efficiency and dynamic output power control. The introduced system combines power from four or more PAs, and overcomes the loss and reactive loading problems of previous outphasing systems. It provides ideally lossless power combining, along with nearly-resistive loading of the individual power amplifiers over a very wide output power range. The theoretical fundamentals underlying the behavior and operation of this new combining system are thoroughly developed. Additionally, a straight-forward combiner design methodology is provided. The prototype design of a 27.12 MHz, four-way power combining and outphasing system is presented, implemented, and its performance is experimentally validated over a 10W-100W (10:1) output power range.

Thesis Supervisor: David J. Perreault
Title: Professor of Electrical Engineering and Computer Science

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Alas, it's done! And most sincerely I must admit that from the very first moment in MIT, to the writing of the very last letter of this thesis, it was one truly incredible journey. I cherish every tiny step of it, and I am deeply grateful for having the opportunity to experience it. However, it was not just a journey of pure academic enlightenment, but in fact - much more than that. It was a true pilgrimage of personal self-discovery that allowed me to glimpse at who I really am, and to uncover my heart's most passionate desires. And to all the people who made it possible, and whose personal journeys fate has intertwined with mine - I humbly thank you!

I can still remember the day I was comfortably slouching in my airplane seat as a freshly-admitted MIT graduate student on my way to the MIT visit week. I was eagerly flipping through the pages of one of professor Perreault's papers on power combining and vividly dreaming of myself one day working on that very same topic with him. And to my surprise, a few months later I was living my dream! It is to you, professor Perreault that I want to express my deepest and most sincere gratitude for your constant guidance, support, and believe in me. Thank you for this one-in-a-lifetime opportunity - without your help, it would have all simply remained just a dream...And of course, how can one imagine it all happening without the friendly LEES "gang" - it is a privilege working with you guys!

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And if I was to end the acknowledgement section right here, it will inevitably result in a request for major thesis revision to the EECS department on behalf of my mother...Unfortunately, a simple "thanks" wouldn't nearly cover it. I thank my dear family for standing by me every step of my journey. It is

to them that I dedicate this thesis: to my father - my patron of wisdom and ultimate health; to my sister - a girl made of fire; and to my mother...To this very day it remains a mystery from where does this woman find the energy to deal with all the crazy adventures of her son. Mother, please forgive me for any white hairs I may have caused you. I secretly hope though that a bigger portion of them is attributed to my sister.

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## Chapter 1

# Introduction

### 1.1. Background

Radio-frequency (RF) power amplifiers are an integral component of many modern systems, and they find wide applicability in a diverse range of applications including RF communications [1], medical imaging [2, 3], industrial heating and processing [4], power conversion [5], and many others. Such power amplifiers (PAs) are often constrained by two important requirements: (1) the ability to provide dynamic control of their output power over a wide range, and (2) the necessity to maintain high efficiency across their operating power range.

For example, Fig. 1-1 shows the envelope of a typical RF signal driving a 7 T MRI RF coil [3]. As can be seen, the output power delivered to the coil is dynamically modulated, with the peaks of the power pulses distributed over nearly a 20 dB of power range. It is highly desired to be able to operate efficiently over such often-occurring, high output power pulses. Although linear power back-off techniques can be utilized to handle the very low output power levels, power-efficient realization of an amplification system that can handle the wide output power modulation range of high-power pulses is a significant challenge for conventional amplification system topologies.

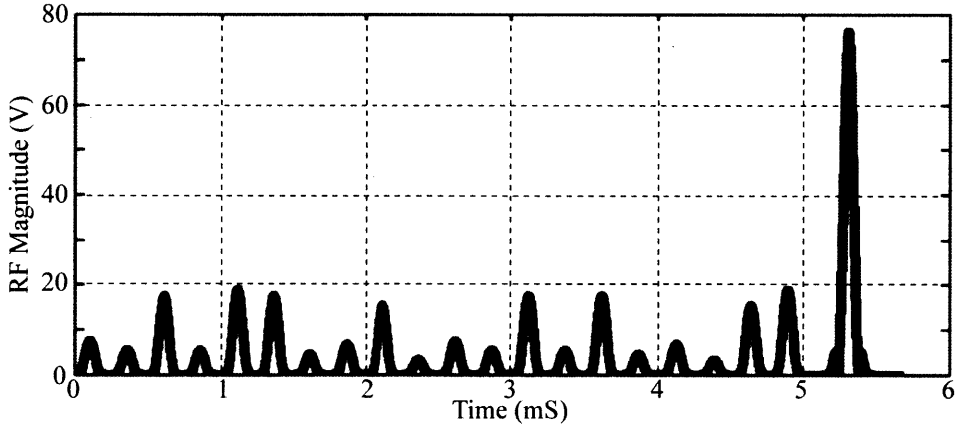



Fig. 1-1: Typical envelope of an RF signal driving a 7 T RF coil in an MRI application [3].

Conventional linear amplifiers such as Class A, AB, B and C allow for a dynamic output power control over a vey wide power range while providing high-fidelity power amplification. However, they can be designed to operate at optimum efficiency at only one particular power level, commonly referred in literature as the output power saturation level. As their output power is backed-off from saturation, their efficiency dramatically degrades. Various efficiency enhancement techniques have been previously proposed to deal with the adverse affects of power back-off on linear PA efficiency [6, 7]. Most such techniques can be categorized as either drain modulation, or load modulation [8, 9]. Drain modulation

techniques such as dynamic envelope tracking and Envelope Elimination and Restoration (EER) ensure that the RF PA operates at or near the saturation level at all times by modulation of its drain voltage [10, 11]. Although drain modulation promises optimal efficiency over a wide operating power range, it requires wide bandwidth, highly-efficient supply regulators; the design of such regulators is very challenging task by itself, especially when wideband modulation is required [11].

On the other hand, load modulation maintains the PA operating at saturation by adjusting the effective loading impedance seen by the PA according to the desired output power [6]. Nevertheless, implementation of the load modulation scheme without introducing extra power loss is not a trivial task. Moreover, most conventional implementations of the load modulation techniques, such as the Doherty amplifier [12-14], allow the PA to operate at optimal efficiency only over a limited output power range (6 dB in the case of a symmetric Doherty amplifier) [15]. The technique explored in this thesis likewise implements a form of load modulation. Some recent digital PA architectures – digital envelope modulator [16-18] and digital switching mixer [19] – offer both excellent linearity and high efficiency at peak output power. Under output power back-off conditions, however, their efficiency degradation is no better than that of a linear class B PA.

Although the discussed techniques reduce PA efficiency degradation with power back-off, their peak efficiency remains low due to the use of linear PAs. On the other hand, switch-mode PAs, e.g., classes D, E, F, E/F, inverse E, inverse F, etc., offer high peak efficiency (100% ideally), but at constant supply voltage can only generate constant envelope signals while remaining in switched mode. Numerous techniques such as drain modulation [20-22], direct digital RF modulation [23, 24], pulse-width or duty-cycle modulation [25], and dynamic load modulation [26] have been proposed to introduce envelope variations in the output of a switching PA. As was already mentioned, drain modulation [22] and its variants [20, 21] require wide bandwidth supply regulators that exhibit poor efficiencies and immensely complicate the system. Direct digital RF modulation [23, 24] demands high sampling speeds and lossy bandpass filters which adversely impact efficiency and add to the overall system cost. Although both duty-cycle [25] and dynamic load modulation [26] techniques offer reasonable efficiency over a narrow operating power range, operation beyond it results in severe efficiency degradation under back-off conditions.

Simultaneously achieving wideband liner power amplification with high average efficiency has been a longstanding challenge, and is the goal of the work presented in this thesis.

## 1.2. The Concept of Power Combining

One technique that has been explored for simultaneously achieving dynamic power control over a wide operating range and high efficiency is that of *outphasing and power combining*. This concept, originally proposed in the 1930's [27], is also sometimes referred to as "Linear Amplification with Non-Linear Components" or LINC [28]. Traditionally, this method (see Fig. 1-2) consists of decomposing the desired input signal to be amplified $S_{in}(t)$ into two phase-modulated signals with constant amplitudes $S_1(t)$ and $S_2(t)$.

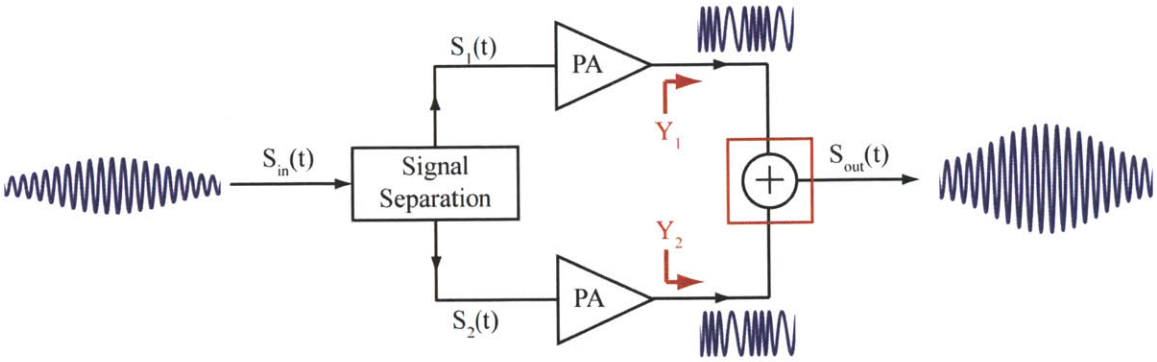



Fig. 1-2: The traditional outphasing and combining method. A desired output envelope $S_{out}$ is created by appropriately outphasing two constant-envelope signals $S_1$ and $S_2$ [29].

These signals are then phase-shifted (outphased), amplified and combined (summed) to yield an amplified version $S_{out}(t)$ of the input signal. Fig. 1-3 shows a phasor representation of the signals. As can be seen, any desirable output signal magnitude can be achieved by simply selecting the appropriate outphasing angle $\theta$. The fact that $S_1$ and $S_2$ are constant-amplitude signals enables the use of highly-efficient PAs including partially- and fully-switched-mode architectures such as classes D [31-32], E [33, 34], F [35-37], E/F [38], $F^{-1}$ [39], $\Phi$ [40, 41], etc. The reason that such PAs can be designed to be highly-efficient is in part due to the fact that they are not required to provide linear output power control.

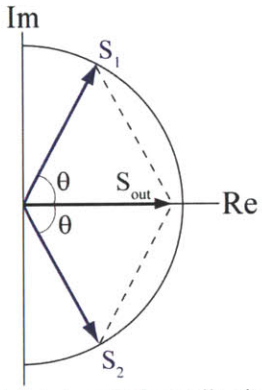



Fig. 1-3: Addition of the two phase-modulated, equal-amplitude signals $S_1$ and $S_2$ in the phasor domain. Any desired $S_{out}$ can be obtained by appropriately selecting the outphasing angle $\theta$ [29].

Although the outphasing and combining methodology above is presented for two PAs, the concept can be generalized for any N number of PAs, where the desired output signal is decomposed into N constant-envelope signals, each being synthesized independently and then combined. A key consideration is how the power combing is carried out, particularly because many high-efficiency power amplifiers are highly sensitive to load impedance variations. Interactions between the PAs, as a result of the combining network, causes the effective admittances ($Y_1$ and $Y_2$ in Fig. 1-2) loading the PAs to vary with outphasing angle (output power) [42-44]. However, variations in PA loading (especially susceptive variations) are often problematic for high efficiency power amplifiers as they give rise to circulating currents, result in

output resonance tank mistuning, and introduce waveform distortions, ultimately leading to degraded PA performance and efficiency. Most conventional combiners can be classified as either *isolating* or *lossless* combiner. A brief overview of the key properties and characteristics of each combiner type follows.

### 1.2.1. The Isolating Combiner

One conventional approach to power combining while eliminating variations in PA loading admittance is the isolating combiner [45]. Fig. 1-4 illustrates the LINC architecture implemented with an isolating combiner [29]. The main advantage of an isolating combiner is that it eliminates PA interactions, and thus provides constant PA loading impedance independent of the outphasing angle. As a consequence of this, each power amplifier operates at a constant output power level. However, only a portion (controlled by outphasing) of the total PA output power is delivered to the load (connected to the summing port Σ of the combiner). The remainder must be instead delivered elsewhere, and usually, it is just dissipated by an "isolation" resistor (connected to the difference port Δ of the combiner). This manifests in rapid efficiency degradation of the combiner as output power is decreased, diminishing the attractiveness of this approach [45]. Previous work has attempted to partially mitigate this problem by replacing the isolation resistor with an AC/DC converter and thus "recycling" a portion of the output difference power back (from the Δ combiner port) to the PA supply [46-48].

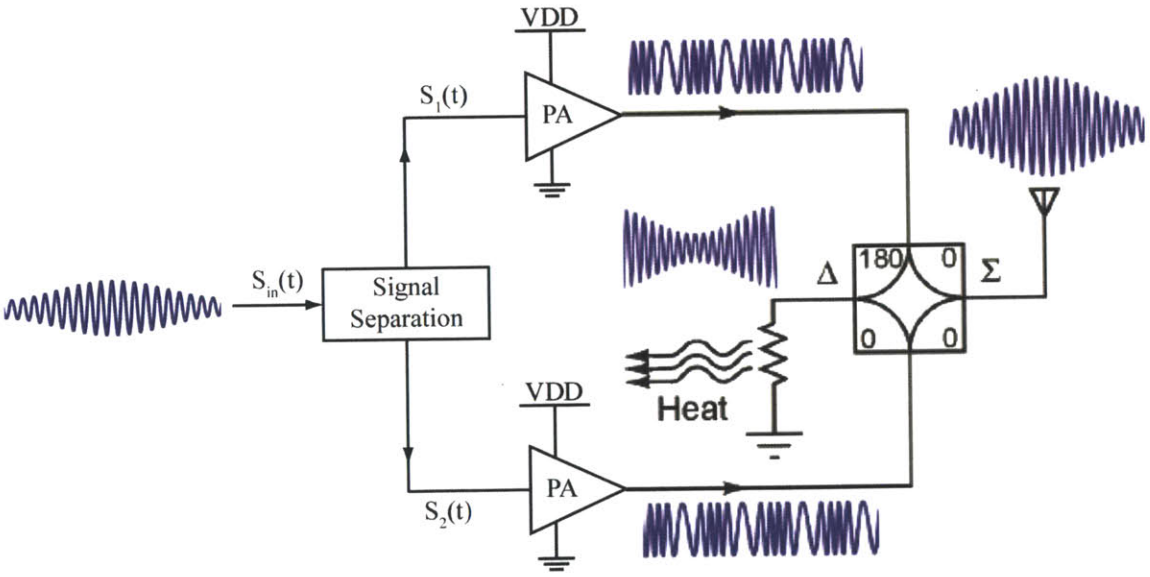



Fig. 1-4: The conventional outphasing architecture implemented with an isolating combiner. A portion of the total constant PA output power is delivered to the load (at the combiner's summing port), while the remainder is dissipated as heat in an "isolation" resistor [29].

As an example implementation of an isolating combiner, consider Fig. 1-5, depicting a simple two-way combiner, also known as a Wilkinson combiner [49, 50]. It comprises two 50 Ω input power ports (1 and 2), combined through two 70.7 Ω quarter wavelength transformers, and a 100 Ω resistor between the two input ports to provide isolation, and make the output port (3) well matched to a 50 Ω load. Provided

that the PAs driving the two combiner input ports are outphased according to Fig. 1-3, they will effectively see a constant resistive loading impedance of 50 Ω.

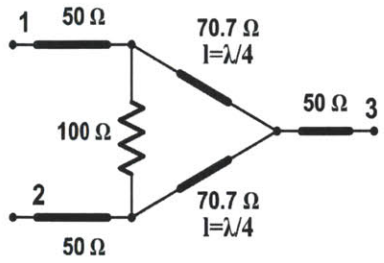



Fig. 1-5: Example implementation of a single-stage Wilkinson combiner [49].

### 1.2.2. Lossless Combining

In contrast to the isolating combiner, the lossless combiner is implemented entirely using only reactive elements such as capacitors and inductors, or transmission lines. Since these elements ideally do not dissipate power, the combining process is ideally lossless, although in reality, some small power loss is unavoidable due to finite quality factor of the components. Fig. 1-6 depicts the simplest two-way lossless combiner comprising a single balun (or "balanced to unbalanced transformer") which is differentially driven by two appropriately outphased PAs.

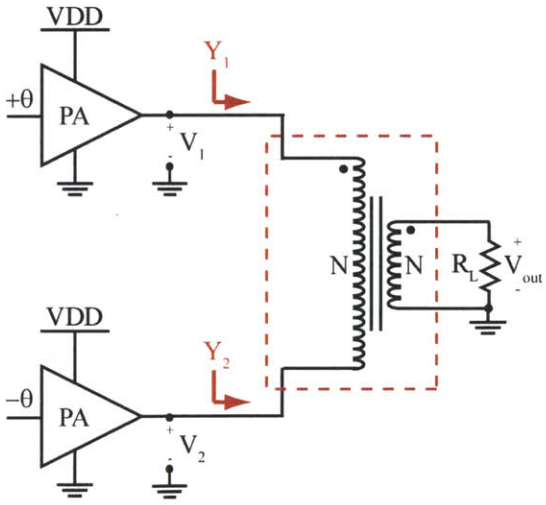



Fig. 1-6: A simple two-way lossless combiner driven by two PAs outphased according to Fig. 1-3. PA interactions cause large susceptive variations in PA loading admittances $Y_1$ and $Y_2$.

To illustrate the operation of this combiner, suppose that the outputs of the PAs are sinusoidal voltage signals with constant amplitude $V_S$, and a respective phase-shift of $\pm\theta$ (see Fig. 1-7 for a phasor diagram). As Fig. 1-7 shows, the magnitude of the output voltage across the load resistor $R_L$ (and hence, the output power $P_{out}$ delivered by the combiner) can be controlled by simply adjusting the outphasing angle $\theta$. It can be shown that output power is given by (1):

$$P_{out} = \frac{2V_S^2 \sin^2(\theta)}{R_L} \tag{1}$$

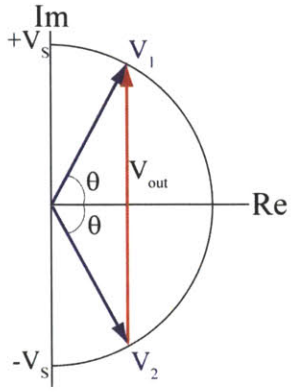



Fig. 1-7: Phasor diagram of the output voltage signals $V_1$ and $V_2$ of the PAs driving the combiner of Fig. 1-6. The PA outphasing angle $\theta$ controls the resulting load voltage $V_{out}$ across $R_L$ and determines output power delivered by combiner.

Output power control can also be understood by considering the behavior of the PA interaction and its effect on PA loading. As a result of PA interactions through the combiner network, the conductive component of the loading admittances $Y_1$ and $Y_2$ "seen" by the PAs vary with outphasing angle. However, since the PAs are biased to provide a constant-amplitude output, modulation of their loading conductance results in modulation of the output power delivered by each PA, and hence, the total output power delivered by the combiner to the load $R_L$. In other words, in a lossless combiner, output power control is achieved by modulation of the loading conductance (dependent on the interaction between the PAs) that the combiner presents to the PAs. It can be shown that for the combiner of Fig. 1-6, the relationship between the loading admittances $Y_1$ and $Y_2$, and the outphasing angle $\theta$ is given by (2):

$$\begin{aligned} Y_1 &= \frac{2}{R_L}\left(\sin^2(\theta) + j\cos(\theta)\sin(\theta)\right) \\ Y_2 &= \frac{2}{R_L}\left(\sin^2(\theta) - j\cos(\theta)\sin(\theta)\right) \end{aligned} \tag{2}$$

A significant drawback of this simple combining approach is that in addition to the modulation of the loading conductance, PA interactions also result in significant susceptive loading variations, which greatly degrade the PA performance and the overall system efficiency. As an example, Fig. 1-6 shows a plot of loading susceptance versus conductance for the PA driving the combiner of Fig. 1-6 with $R_L = 20.4\ \Omega$. As can be seen, the susceptive component varies over more than 50% of the range over which the PA loading conductance is modulated.

The large variations in PA loading susceptance can be partially compensated by connecting additional reactive components $\pm jX_C$ to the PA output nodes (see Fig. 1-8). This configuration is also known as the Chireix combiner [27, 42, 43, 45, 51] after its developer, who introduced it in the 1930's [27]. It can be shown that the loading admittances $Y_1$ and $Y_2$, and the combiner output power $P_{out}$ as a function of PA outphasing angle $\theta$ are given respectively by (3) and (4):

$$P_{out} = \frac{2V_S^2 R_L \sin^2(\theta)}{X_C^2} \tag{3}$$

$$Y_1 = \frac{2}{R_L}\left(\sin^2(\theta) + j\left(\cos(\theta)\sin(\theta) - \frac{R_L}{X_C}\right)\right)$$

$$Y_2 = \frac{2}{R_L}\left(\sin^2(\theta) - j\left(\cos(\theta)\sin(\theta) - \frac{R_L}{X_C}\right)\right) \tag{4}$$

Indeed, as can be seen from (4), the susceptive components have been shifted by an amount proportional to the ratio of $R_L$ to $X_C$. Fig. 1-9 shows a susceptance/conductance plot for various Chireix example designs with $R_L$ and $X_C$ selected to reflect the same loading conductance modulation range for all designs. As seen, the susceptive portions of the PA loading admittances are only zero for at most two output power levels, and become large outside of a limited power range. Although the susceptive variations of the Chireix combiner are smaller compared to those of the uncompensated combiner of Fig. 1-6, they are still problematic for high-efficiency application requiring wide output power range [42-44].

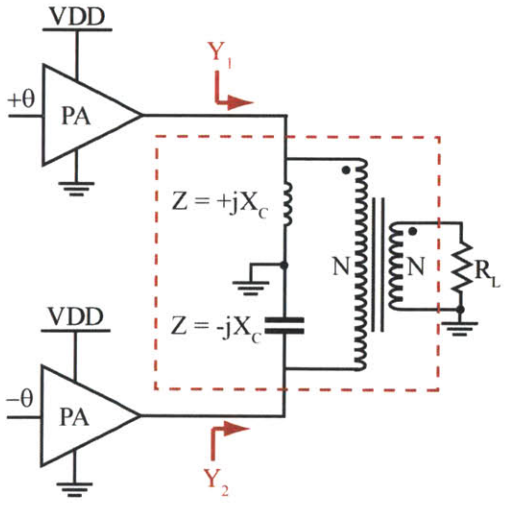



Fig. 1-8: A simple two-way combiner including $\pm jX_C$ reactances to partially compensate for susceptive variations in PA loading admittances $Y_1$ and $Y_2$. This combiner topology was originally proposed in the 1930's by Chireix [29].

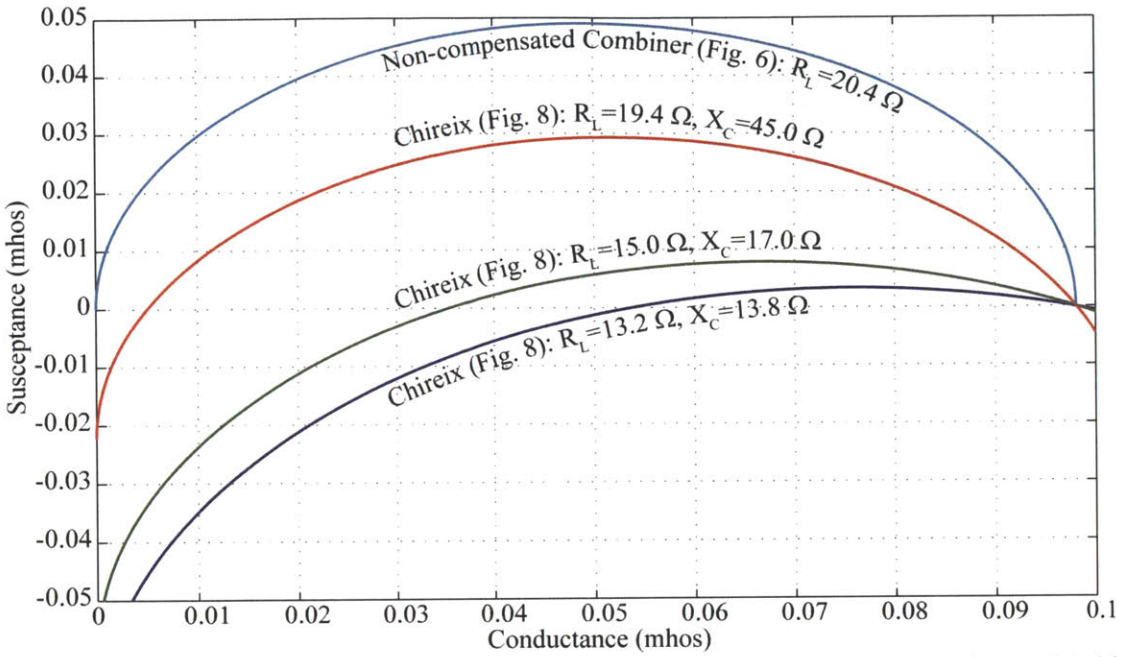



Fig. 1-9: Susceptive versus conductive component of the loading admittance $Y_1$ seen by the top PA driving the combiners of Fig. 1-6 and Fig. 1-8. Although only $Y_1$ is plotted, $Y_2$ is the complex conjugate of $Y_1$.

## 1.3. Thesis Objectives and Organization

The primary objective of this thesis is to describe the development of a new multi-way power combing and outphasing system that provides ideally lossless power combining from four or more PAs, along with nearly-resistive loading of the individual power amplifiers over a very wide output power range. More specifically, this thesis aims to achieve the following key objectives

- Describe the theoretical fundamentals necessary for understanding and analyzing the operation of the proposed power combiner,
- Present a design methodology for designing the combiner according to specific performance specifications,
- Develop outphasing control strategies for controlling the combiner's output power,
- Experimentally evaluate the performance of the proposed combiner, and validate the effectiveness of the outphasing control strategies to control the output power of the combiner.

Following this introductory chapter, Chapter 2 discusses the fundamentals of operation of the proposed power combiner, addressing combiner synthesis, combiner port characteristics, outphasing

control, design methodologies, and various implementation topologies. The implementation of an actual power combining system prototype is presented in Chapter 3, while Chapter 4 evaluates its performance and assesses the effectiveness of the proposed combining approach. Chapter 5 presents a transmission-line implementation of the combiner suitable for power combining applications in the UHF band. The thesis is concluded in Chapter 6 with remarks on possible areas of future development.

The appendices following the thesis include associated derivations referenced in the text, some generalized theoretical developments on multi-way power combining, computer code employed in system simulation, printed circuit board schematics and artwork, and embedded firmware code.

## Chapter 2

# Power Combiner Fundamentals

This chapter develops and presents the fundamentals of operation of the new outphasing power combining architecture. It aims to layout necessary theoretical foundation and provide in-depth understanding of the behavior and the principles of operation of the combiner. Furthermore, useful techniques and methods are described which greatly facilitate future combiner design and analysis.

As a first step, the notion of multi-stage resistance compression networks is introduced. Although a seemingly unrelated topic at first, it is shown how the design and behavior of multi-stage compression networks can be effectively utilized in the synthesis of ideally lossless power combiners and in the derivation of their corresponding outphasing control laws. Following subsections discuss important input-port and output-port combiner characteristics along with various outphasing techniques to control combiner output power and their loading affect on the driving power amplifiers. A methodology is presented which allows for a straightforward combiner design based on given system performance specifications. The last two subsections present various topological circuit implementations of the combiner and their effect on non-ideal combining losses.

## 2.1. Overview of Resistance Compression Networks

Resistance Compression Networks (RCNs) are a class of lossless interconnection networks for coupling a source to a set of matched (but variable) resistive loads [46, 52, 53] at a particular operating frequency. Fig. 2-1 depicts one basic RCN and its operating characteristics. As the resistances $R_o$ in Fig. 2-1 vary together over a range geometrically-centered on X, the input impedance of the network is entirely resistive and varies over a much smaller range compared to $R_o$, i.e. loading resistance variations are compressed. In particular, it can be shown (5) that the input impedance $R_{in}$ is resistive at the operating frequency and it is a function of the load resistances $R_o$ [29, 46, 52, 53]:

$$R_{in} = \frac{R_o^2 + X^2}{2R_o} \tag{5}$$

As the load resistances $R_o$ vary over the range [X/b, bX], the input resistance varies over the range [X, kX], where k and b are related by (6):

$$k = \frac{1+b^2}{2b} \quad \text{and} \quad b = k + \sqrt{k^2 - 1} \tag{6}$$

For example, if the loading resistances $R_o$ vary simultaneously over a range of 5 Ω to 500 Ω (a factor of b = 10 variation from a 50 Ω nominal resistance), then $R_{in}$ varies only over a range of 50 Ω to 252.5 Ω.

Because the input impedance is resistive and varies over a much smaller range than the matched load resistances $R_o$, RCN networks offer numerous advantages in applications such as resonant rectifiers and dc-dc converters [46, 52, 53].

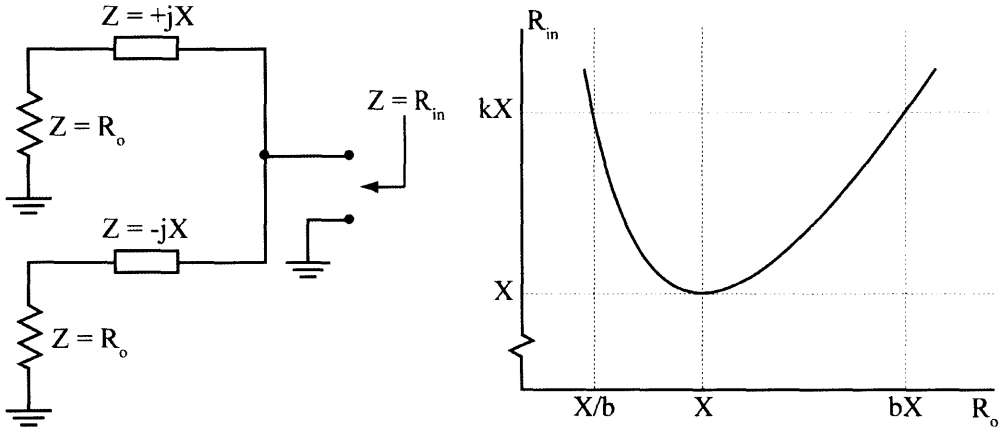



Fig. 2-1: (Left) a basic resistance compression network (RCN) and (right) its resistive input impedance $R_{in}$ as a function of the matched load resistance value $R_o$. As the resistances $R_o$ vary together over a range geometrically-centered on X, the input impedance is resistive and varies over a much smaller range than $R_o$.

The RCN of Fig. 2-1 is a narrow-band network – it is designed for operation at a particular frequency at which the values of the capacitive and inductive RCN impedances are tuned to ±jX. Suppose that this RCN is now driven by a sinusoidal voltage source $V_L$ at its operating frequency. Then, it can be shown that the voltage waveforms $V_A$ and $V_B$ across the loads $R_o$ have equal magnitudes and are symmetrically phase-shifted by ±ϕ with respect to $V_L$ (see Fig. 2-2) according to (7) and (8):

$$\begin{bmatrix} V_A \\ V_B \end{bmatrix} = V_L \frac{R_o}{\sqrt{R_o^2 + X_1^2}} \begin{bmatrix} e^{-j\phi} \\ e^{+j\phi} \end{bmatrix} \tag{7}$$

$$\phi = tan^{-1}\left(\frac{X_1}{R_o}\right) \tag{8}$$

The RCN discussed above can be thought of as a basic single-stage compression network. However, even higher degrees of resistance compression (smaller input resistance variations for the same loading resistance variation) can be achieved by constructing multiple-stage compression networks. Fig. 2-3 (left) shows an example implementation of a two-stage RCN (other possible implementations exist). The simultaneous resistance variations in the four loads $R_o$ is first compressed by a pair of single-stage RCNs. In turn, their simultaneously varying effective input resistances $R_{in,1}$ are further compressed by another single-stage RCN.

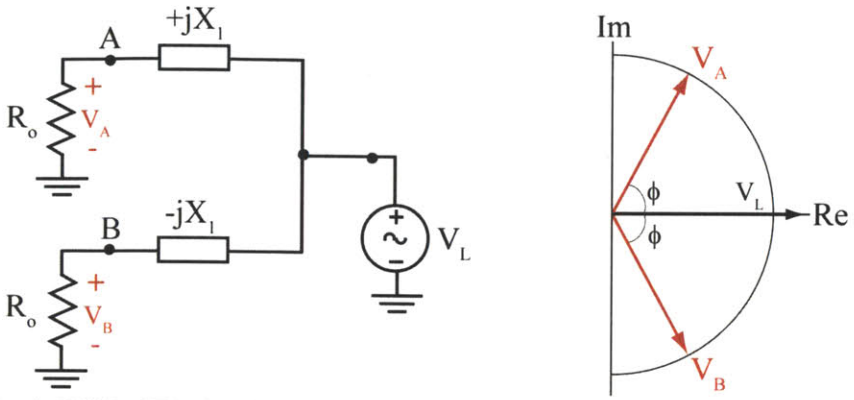



Fig. 2-2: The basic RCN of Fig. 2-1 driven by a sinusoidal voltage source $V_L$ (left) and the phasor diagram of the voltages $V_A$ and $V_B$ across the loading resistors (right).

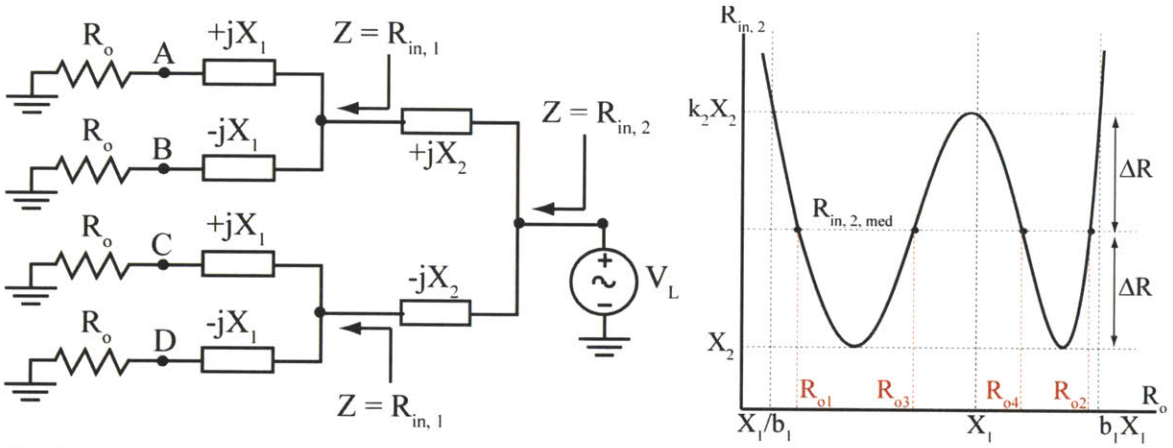



Fig. 2-3: A second-order resistance compression network driven by a sinusoidal voltage source $V_L$ at its operating frequency (left), and its overall resistance compression characteristic (right).

The design of the RCN of Fig. 2-3 is now considered. The following subsection shows how this RCN relates to the proposed combining system. Suppose it is desired to design the RCN of Fig. 2-3 to provide an input resistance $R_{in,2}$ within $\pm\Delta R$ of a desired median value $R_{in,2,med}$ while maximizing the range over which $R_o$ can vary [60]. First, select a value $k_2$ (input resistance ratio of stage 2) of:

$$k_2 = \frac{R_{in,2,med} + \Delta R}{R_{in,2,med} - \Delta R} \tag{9}$$

and choose a second stage reactance magnitude of

$$X_2 = \frac{2R_{in,2,med}}{k_2 + 1} \tag{10}$$

Next, the reactance magnitude $X_1$ of the first stage is selected to provide compression into a range that makes best use of the second stage. Note that in order to limit $R_{in,2}$ variations within the specified design range of $R_{in,2,med} \pm \Delta R$ , variations of $R_{in,1}$ must be constrained to a range of $[X_2/b_2;\ X_2 b_2]$. Since the effective resistance $R_{in,1}$ seen at the inputs of the first stage has a minimum value of $X_1$, to maximize the range of $R_o$ over which desired compression is achieved, select $X_1$ to be:

$$X_1 = \frac{X_2}{b_2} \tag{11}$$

where $b_2$ is determined from $k_2$ according to (6). $R_{in,1}$ has a maximum value of $k_1 X_1 = b_2 X_2$, from where the value of $k_1$ can be determined. Thus, the desired degree of compression can be achieved for an $R_o$ operating range of $[X_1/b_1;\ b_1 X_1]$, with $b_1$ given by (6). Equivalently, it can be shown that $b_1$ can be computed directly from $k_2$ as per (12):

$$b_1 = \left(k_2 + \sqrt{k_2^2 - 1}\right)^2 + \sqrt{\left(k_2 + \sqrt{k_2^2 - 1}\right)^4 - 1} \tag{12}$$

Fig. 2-3 depicts the variation of the input resistance $R_{in,2}$ as a function of the load resistance $R_o$ when the compression network is designed according to the method outlined above. This particular resistance compression characteristic is the result of selecting the network reactances $X_1$ and $X_2$ as described; the network exhibits far greater degree of resistance compression than its single-stage counterpart described earlier. For instance, the two-stage RCN allows for input resistance compression within ±2.5% of the desired median value (versus ±30.5% for the single-stage RCN) over a 12:1 ratio in load resistance $R_o$ modulation. Note that other types of compression stages can yield similar performance [52, 53]. Moreover, even greater degree of resistance compression (or similar input resistance deviations over a wider load modulation range) can be achieved with more stages. A detailed methodology for designing and synthesizing a general multi-stage RCN optimized for maximum resistance compression is presented in Appendix A along with design examples and summary of performance characteristic for single-stage, two-stage, and three-stage RCNs.

It is useful to be able to determine the value of $R_o$ for which $R_{in,2} = R_{in,2,med}$. This can be easily done by employing the RCN compression equation (5), expressing $R_{in,2}$ as a function of $R_o$:

$$R_{in,2} = \frac{R_{in,1}^2 + X_2^2}{2R_{in,1}} = \frac{\left(\frac{R_o^2 + X_1^2}{2R_o}\right) + X_2^2}{2\left(\frac{R_o^2 + X_1^2}{2R_o}\right)} \tag{12.1}$$

Solving for $R_{in,2} = R_{in,2,med}$ results in four distinct values of $R_o$ (for the case of the second-order RCN) given by (12.2)-(12.5):

$$R_{o1} = \left( R_{in,2,med} + \sqrt{R_{in,2,med}^2 - X_2^2} - \sqrt{2R_{in,2,med}^2 - X_1^2 - X_2^2 + \frac{2R_{in,2,med}^3 - 2R_{in,2,med}X_2^2}{\sqrt{R_{in,2,med}^2 - X_2^2}}} \right) \quad (12.2)$$

$$R_{o2} = \left( R_{in,2,med} + \sqrt{R_{in,2,med}^2 - X_2^2} + \sqrt{2R_{in,2,med}^2 - X_1^2 - X_2^2 + \frac{2R_{in,2,med}^3 - 2R_{in,2,med}X_2^2}{\sqrt{R_{in,2,med}^2 - X_2^2}}} \right) \quad (12.3)$$

$$R_{o3} = \left( R_{in,2,med} - \sqrt{R_{in,2,med}^2 - X_2^2} - \sqrt{2R_{in,2,med}^2 - X_1^2 - X_2^2 - \frac{2R_{in,2,med}^3 - 2R_{in,2,med}X_2^2}{\sqrt{R_{in,2,med}^2 - X_2^2}}} \right) \quad (12.4)$$

$$R_{o4} = \left( R_{in,2,med} - \sqrt{R_{in,2,med}^2 - X_2^2} + \sqrt{2R_{in,2,med}^2 - X_1^2 - X_2^2 - \frac{2R_{in,2,med}^3 - 2R_{in,2,med}X_2^2}{\sqrt{R_{in,2,med}^2 - X_2^2}}} \right) \quad (12.5)$$

It will be appreciated in the following subsection to know the load voltages $V_A$-$V_D$ in terms of the drive voltage $V_L$. It can be shown by employing straightforward phasor analysis at the RCN's operating frequency that these voltages are related according to (13)-(15).

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_L \frac{\sqrt{R_o^2 + X_1^2}}{2\sqrt{\left(\frac{R_o^2 + X_1^2}{2R_o}\right)^2 + X_2^2}} \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{+j\phi}e^{-j\theta} \\ e^{-j\phi}e^{+j\theta} \\ e^{+j\phi}e^{+j\theta} \end{bmatrix} \quad (13)$$

$$\theta = tan^{-1}\left(\frac{2R_oX_2}{R_o^2 + X_1^2}\right) \quad (14)$$

$$\phi = tan^{-1}\left(\frac{X_1}{R_o}\right) \quad (15)$$

Fig. 2-4 illustrates their phasor relationship. Similarly to the single-stage RCN, it can be seen that $V_A$-$V_D$ have the same magnitude and symmetrical phase shifts with respect to $V_L$ (coincident with the the real axis).

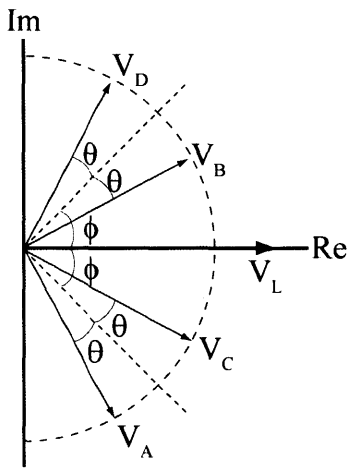



Fig. 2-4: Phasor representation of the load voltages $V_A$-$V_D$ of the RCN of Fig. 2-3 symmetrically phase shifted with respect to the driving voltage $V_L$.

## 2.2. Power Combiner Synthesis

The previous subsection discussed the concept of multi-stage resistance compression networks, and examined in detail the behavior and design of a single-stage and two-stage RCNs. This subsection demonstrates how the design of such compression networks may be employed in synthesizing the proposed power combining system.

Consider the two-stage RCN of Fig. 2-3 driven by a voltage source $V_L$. Suppose now that the sign of every reactive and resistive element is negated. Neglecting the impact upon the natural response of the circuit, the sinusoidal steady-state behavior of the transformed circuit would have all current flow directions reversed, while preserving the node voltage relationships of the original circuit, thus yielding reversed power flow (i.e. from the – now negative – resistors to the voltage source $V_L$). (The validity of this fact can be shown by taking the original circuit of Fig. 2-3 and applying to it type-I, followed by type-III time reversal dualities according to [54, 55].) The ratio of the voltage $V_L$ to the current flowing into the source would be that of $R_{in,2}$ of the original compression network, which is close to the value of $R_{in,2,med}$. Likewise, the voltages across the now-negative resistors would be respectively equivalent to the ones in the original network (13), and currents proportional to these voltages would flow into the network (i.e. the apparent impedances seen looking into the network ports to which the negative resistances are connected would be resistive with values $|R_o|$) [60].

To develop a power combining and outphasing system, one may take advantage of the above observations. In particular, replace the source $V_L$ in Fig. 2-3 with a load resistance $R_L = R_{in,\,2,\,med}$ and replace the resistors $R_o$ with voltage sources (or power amplifiers in practice). This leads directly to the power combiner of Fig. 2-5. It has four input power ports A-D (driven by PAs) and a single output power port terminated at a desired and well-known load at the operating frequency. The combiner provides ideally lossless power combining in the sense that the reactive components it comprises are ideally lossless. Note

that, just as the compression network, the combiner is also a narrow-band network. Its reactances are tuned to a particular value (determined by design) at the combiner's operating frequency.

By controlling the phases of the driving sources $V_A$-$V_D$ to match (or at least approximately) the A-D node voltage relationships in the original two-stage resistance compression network (see Fig. 2-4), one can obtain power control over a wide range while preserving nearly resistive loading of the sources. The following subsections develop and discuss in detail the actual outphasing techniques for controlling the combiner's output power and the particular advantages and disadvantages associated with each one.

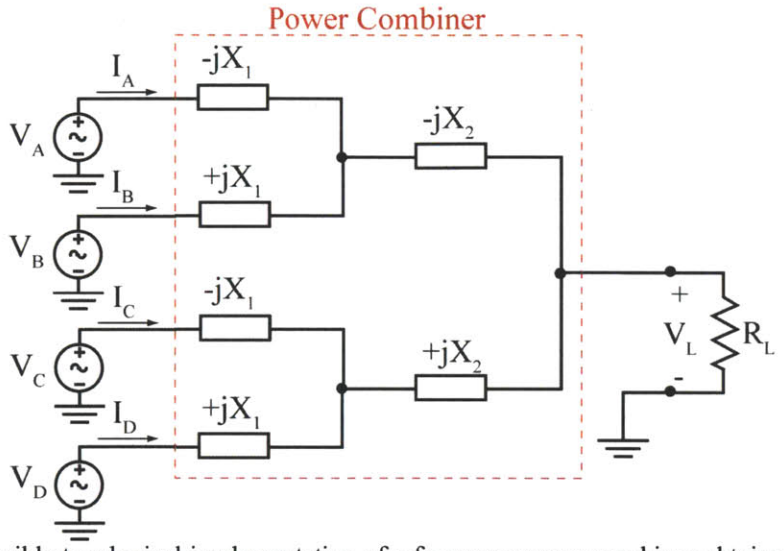



Fig. 2-5: One possible topological implementation of a four-way power combiner obtained by negating the reactances of the RCN of Fig. 2-3, replacing the $R_o$ loads with PAs, and replacing the RCN driving source $V_S$ with a combiner termination load $R_L$.

While the employed circuit transformations considered above do not lead to precise duality between RCNs and the proposed power combining network, they provide the means to develop effective outphasing and power combing systems [29]. These same transformations can be applied to a general N-stage RCN (having $2^N$ loads) to arrive at a respective $2^N$-way power combining network (combing power from $2^N$ PAs). Interestingly, when this transformation is applied to the single-stage RCN, one obtains a topological variation of the Chireix combiner of Fig. 1-8. Although the main portion of the work disclosed in this thesis considers the four-way combiner of Fig. 2-5, the concepts, design techniques and outphasing control methodologies developed herein can be easily adapted for any multi-way combiner. Appendix B demonstrates how to do so for an eight-way combiner. Due to the non-ideal lossy character of the combiner reactances, and the rapidly-growing system complexity, one would rarely consider in practice expanding the proposed combiner architecture to provide power combining from more than eight PAs. Moreover, it is worth recognizing that the "binary-tree" structure shown in Fig. 2-5 is not the only possible topological implementation of the combiner; various topological variations exist. Later subsections enumerate some of these variations and discuss their effect on combining power losses for the case of the four-way combiner. Appendix B further extends these topological variations to the case of the eight-way combiner.

## 2.3. Input-Port Combiner Characteristics

In order to understand the behavior of the proposed combiner, it is important to examine the current/voltage characteristic at the network's input ports and the loading it presents to the PAs that drive it. Consider the four-way combiner of Fig. 2-5 terminated with a load $R_L$. To simplify analysis, the PAs driving the combiner are modeled here as ideal sinusoidal voltage sources $V_A$-$V_D$ at the combiner's operating frequency with amplitude $V_S$ and phasor relationship as shown in Fig. 2-4. Simple AC analysis reveals that the relationship between the input terminal voltages $V_A$-$V_D$ and currents $I_A$-$I_D$ is given by (16), where $\gamma = R_L/X_1$, $\beta = X_2/X_1$ [29].

$$\begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \end{bmatrix} = Y \cdot \vec{V} = X_1^{-1} \begin{bmatrix} \gamma + j(1-\beta) & -\gamma + j\beta & \gamma & -\gamma \\ -\gamma + j\beta & \gamma - j(\beta+1) & -\gamma & \gamma \\ \gamma & -\gamma & \gamma + j(\beta+1) & -\gamma - j\beta \\ -\gamma & \gamma & -\gamma - j\beta & \gamma + j(\beta-1) \end{bmatrix} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} \tag{16}$$

Moreover, the input terminal voltages (Fig. 2-4) can be further expressed by (17). Note that their phases have been chosen identical to those of the RCN's load voltages (13).

$$\vec{V} = \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{+j\phi}e^{-j\theta} \\ e^{-j\phi}e^{+j\theta} \\ e^{+j\phi}e^{+j\theta} \end{bmatrix} \tag{17}$$

By combining (16) and (17), one can determine the effective input admittances the combiner network presents to each of the PAs (18)-(21). The effective admittance at a combiner input port is the complex ratio of current to voltage at the port with all sources (PAs) active. The effective admittances represent the admittances "seen" by the PAs when they are operating under outphasing control [29].

$$\begin{aligned} Y_{eff,A} = {} & X_1^{-1}(\gamma - \gamma cos(2\phi + 2\theta) - \gamma cos(2\phi) + \gamma cos(2\theta) - \beta sin(2\phi)) \\ & + jX_1^{-1}(1 - \beta - \gamma sin(2\phi + 2\theta) - \gamma sin(2\phi) + \gamma sin(2\theta) + \beta cos(2\phi)) \end{aligned} \tag{18}$$

$$\begin{aligned} Y_{eff,B} = {} & X_1^{-1}(\gamma - \gamma cos(2\theta - 2\phi) - \gamma cos(2\phi) + \gamma cos(2\theta) + \beta sin(2\phi)) \\ & + jX_1^{-1}(-1 - \beta - \gamma sin(2\theta - 2\phi) + \gamma sin(2\phi) + \gamma sin(2\theta) + \beta cos(2\phi)) \end{aligned} \tag{19}$$

$$\begin{aligned} Y_{eff,C} = {} & X_1^{-1}(\gamma - \gamma cos(2\theta - 2\phi) - \gamma cos(2\phi) + \gamma cos(2\theta) + \beta sin(2\phi)) \\ & - jX_1^{-1}(-1 - \beta - \gamma sin(2\theta - 2\phi) + \gamma sin(2\phi) + \gamma sin(2\theta) + \beta cos(2\phi)) \end{aligned} \tag{20}$$

$$\begin{aligned} Y_{eff,D} = {} & X_1^{-1}(\gamma - \gamma cos(2\phi + 2\theta) - \gamma cos(2\phi) + \gamma cos(2\theta) - \beta sin(2\phi)) \\ & - jX_1^{-1}(1 - \beta - \gamma sin(2\phi + 2\theta) - \gamma sin(2\phi) + \gamma sin(2\theta) + \beta cos(2\phi)) \end{aligned} \tag{21}$$

It is important to consider the effective input admittance instead of the Thevinin input admittance at a particular port, as the interaction of the PAs has a substantial effect on their actual loading. It is interesting to note that as a result of the combiner structure and the employed PA outphasing relationship, the effective input admittances at ports A/D, and C/ B are respectively complex conjugates. As can be seen from (18)-(21), the loading of the PAs is a strong function of the outphasing angles $\theta$ and $\phi$, and varies with outphasing (output power control). The actual admittance characteristic over the combiner's operating power range is specific to the particular outphasing control law employed (the method used for selecting $\theta$ and $\phi$ for a particular output combiner power level). These control laws and their affect on the PAs loading are discussed in detail in Section 2.5. Moreover, it will be recognized that the exact expressions for the effective input admittances depend on the number of PAs from which power is combined. Although this section provides the expressions for the four-way combiner, Appendix B derives similar expressions for the eight-way combiner.

## 2.4. Output Power Control

It is useful to know the load voltage $V_L$ and the output power $P_{out}$ that the combiner delivers to the load $R_L$ (see Fig. 2-5) for a given pair of outphasing control angles [$\theta$; $\phi$]. By employing straightforward linear circuit analysis techniques, it can be shown that the load voltage $V_L$ is given by (22):

$$V_L = j\frac{R_L}{X_1}(V_B + V_D - V_A - V_C) \tag{22}$$

Furthermore, as a result of the adopted voltage phase relationship of Fig. 2-4, the above equation reduces to (23), from where the output power $P_{out}$ delivered to the combiner load $R_L$ is easily determined (24).

$$V_L = -\frac{4R_L}{X_1} V_S \sin(\phi)\cos(\theta) \tag{23}$$

$$P_{out} = \frac{V_L^2}{2R_L} = \frac{8R_L V_S^2}{X_1^2}\sin^2(\phi)\cos^2(\theta) \tag{24}$$

Equation (24) is of great importance and value as it concisely expresses the exact relationship between the output power delivered to the load $R_L$ and any pair of outphasing control angles [$\theta$; $\phi$]. This equation holds on the assumption that the combiner inputs are each driven with the specified voltage. It is the fundamental basis for deriving the various outphasing control laws in the following subsection. As can be seen from (24), output power may be controlled either through phase-modulation (adjusting the angles $\theta$ and $\phi$), or through amplitude-modulation (adjusting the PA drive signal amplitude $V_S$), or through both. In

practice, one may choose to employ simultaneously both phase- and amplitude-modulation to achieve an even wider operating output power range.

It is readily observed from (24) that the maximum output power deliverable to the load by the power combiner, termed here the saturated output power $P_{out,sat}$, is given by (25), and corresponds to $\theta = 0°$ and $\phi = 90°$. Although (25) is valid only for the four-way combiner, the only difference between it and that for the general N-way combiner is the leading numeric constant. Appendix B derives the expression for output power for the eight-way combiner.

$$P_{out,sat} = \frac{8R_L V_S^2}{X_1^2} \tag{25}$$

## 2.5. Outphasing Control Strategies

As described in the previous subsection, the output power of the proposed power combiner may be controlled either by modulating the drive amplitude of the power amplifiers, or by appropriately adjusting their phase shift (outphasing). For the four-way combiner of Fig. 2-5 with PAs outphased according to Fig. 2-4, the output power $P_{out}$ is given by (24). As can be seen from (24), for a particular PA drive amplitude $V_S$, there are infinite many possible control angle pairs $[\theta, \phi]$ that will result in the same output power level. Thus, an additional constraint can be specified on $\theta$ and $\phi$ to allow for the selection of a particular control angle pair. Depending on the nature of the constraint, many possible outphasing control methodologies emerge. This subsection details several control methodologies and their key characteristics which are of particular relevance to various practical applications.

### 2.5.1. Inverse Resistance Compression Network (IRCN) Control

This outphasing control strategy results by analogy of (approximate) reverse operation of the original resistance compression network, i.e. the PAs driving the combiner are appropriately outphased so that their terminal voltage characteristic matches the one of the load resistances in the original RCN. As a result, the power delivered to load $R_L$ driven by the power combiner is approximately equivalent to the power that would be delivered by a power source driving the original RCN and having the same terminal voltage as $R_L$. This outphasing control method yields desirable loading (almost entirely conductive effective input admittance) of the PAs. Moreover, due to this control method, the necessary outphasing control angles can be computed conveniently via a set of analytical expressions which are valid over the entire output power operating range of the combiner assuming voltage-source drive of the combiner.

For the case of the four-way power combiner of Fig. 2-5, the outphasing control angles $\theta$ and $\phi$ for a particular load $R_L$ and PA voltage drive amplitude $V_S$ are given by (26) with the variable $R_o$ determined based on the desired combiner output power $P_{out}$ (27).

$$\theta = tan^{-1}\left(\frac{2R_oX_2}{R_o^2+X_1^2}\right) \text{ and } \phi = tan^{-1}\left(\frac{X_1}{R_o}\right) \tag{26}$$

$$R_o = \sqrt{\frac{4R_LV_S^2}{P_{out}} - X_1^2 - 2X_2^2 + 2\sqrt{\frac{4R_L^2V_S^4}{P_{out}^2} - \frac{4R_LV_S^2X_2^2}{P_{out}} + X_1^2X_2^2 + X_2^4}} \tag{27}$$

As an example of the IRCN outphasing control, Fig. 2-6 depicts the loading admittance characteristic of each of the A-D PAs driving the combiner of Fig. 2-5 versus output power back-off by outphasing. For this example, the combiner has been designed to operate over approximately a 10 dB output power back-off and drive a 50 Ω load ($R_L$ = 50 Ω, $X_1$ = 36.69 Ω, $X_2$ = 48.97 Ω). The actual output power level is proportional to the square of the PA drive amplitude $V_S$. (Selecting the appropriate values for the combiner reactances $X_1$ and $X_2$ to achieve operation over a specified output power range is detailed in Section 2.7.)

As can be seen from Fig. 2-6, the PA loading conductance is modulated accordingly with output power, while the susceptance and the admittance phase variations are limited to approximately 2.5 mS and 5° respectively over the intended operating range. For this particular example, the susceptive component of the combiner's input admittances rapidly increase for more than 10 dB output power back-off, or for operation at power levels above 0 dB. In fact, it can be shown in general from (18)-(21) and (26) that for zero output power ($P_{out}$ = 0), all PA voltages $V_A$-$V_D$ are in phase ($\theta = 0°$, $\phi = 0°$), and the effective input admittances (purely susceptive) are:

$$\begin{aligned} Y_{eff,A} &= Y_{eff,C} = jX_1^{-1} \\ Y_{eff,B} &= Y_{eff,D} = -jX_1^{-1} \end{aligned} \tag{28}$$

On the other hand, when $\theta = 0°$ and $\phi = 90°$, the output power saturates to $P_{out,sat}$ (25) and the PAs are loaded with an admittances having significant susceptive components given by (29), where $\gamma = R_L/X_1$, $\beta = X_2/X_1$.

$$\begin{aligned} Y_{eff,A} &= X_1^{-1}(4\gamma + j(1-2\beta)) \\ Y_{eff,B} &= X_1^{-1}(4\gamma + j(-1-2\beta)) \\ Y_{eff,C} &= X_1^{-1}(4\gamma - j(-1-2\beta)) \\ Y_{eff,D} &= X_1^{-1}(4\gamma - j(1-2\beta)) \end{aligned} \tag{29}$$

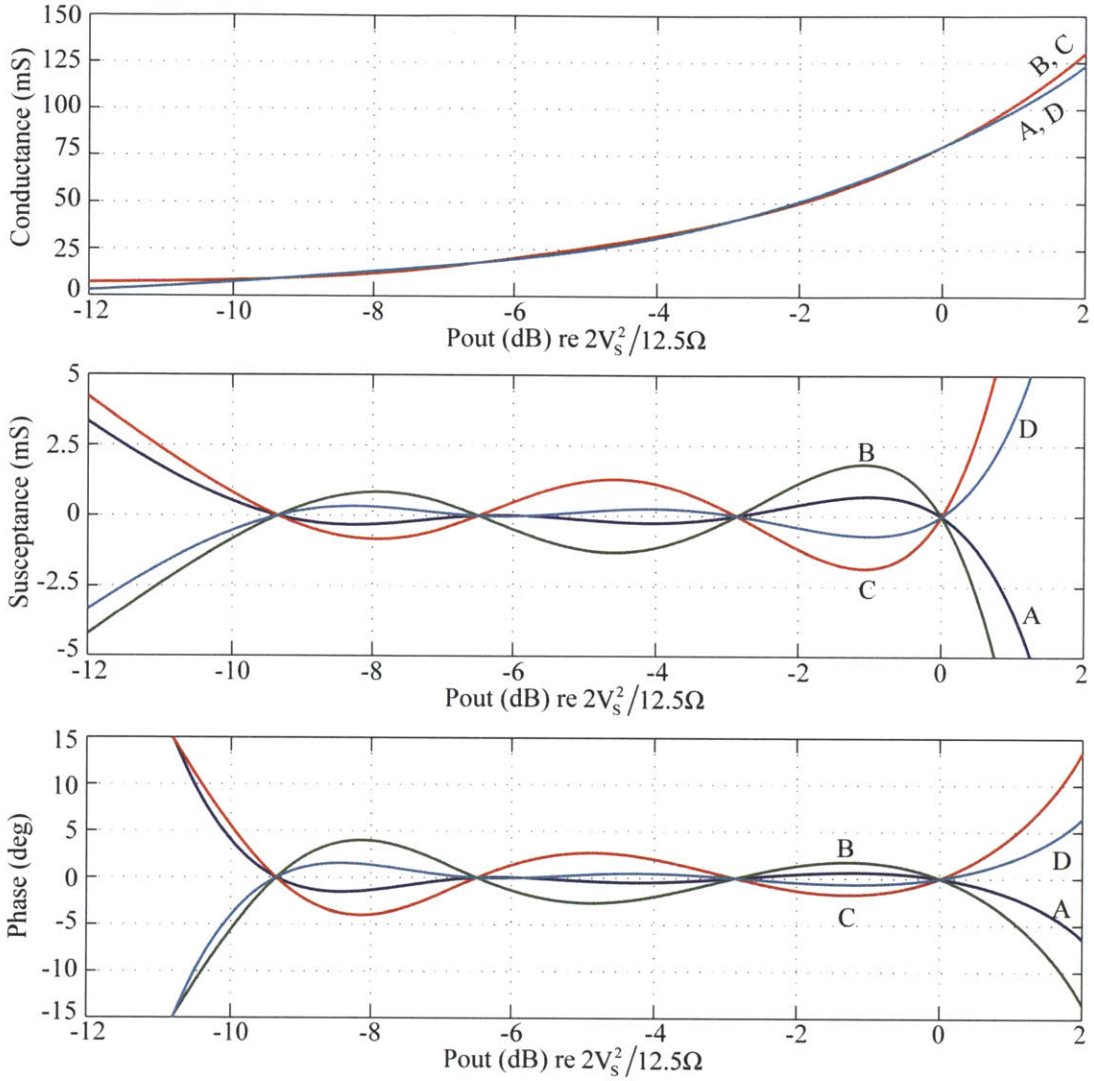



Fig. 2-6: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way combiner of Fig. 2-5 with $R_L = 50\ \Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$ as a result of IRCN outphasing control.

One can also observe from Fig. 2-6 that all four susceptive components of the combiner's input admittances vanish to zero at four distinct output power levels (termed here the *zero-points*). The output power corresponding to these zero-points can be computed according to (30)-(33).

$$P_{out,zp1} = 2V_S^2\left(R_L + \sqrt{R_L^2 - X_2^2} - \sqrt{2R_L^2 - X_1^2 - X_2^2 + \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \tag{30}$$

$$P_{out,zp2} = 2V_S^2\left(R_L + \sqrt{R_L^2 - X_2^2} + \sqrt{2R_L^2 - X_1^2 - X_2^2 + \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \tag{31}$$

$$P_{out,zp3} = 2V_S^2\left(R_L - \sqrt{R_L^2 - X_2^2} - \sqrt{2R_L^2 - X_1^2 - X_2^2 - \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (32)$$

$$P_{out,zp4} = 2V_S^2\left(R_L - \sqrt{R_L^2 - X_2^2} + \sqrt{2R_L^2 - X_1^2 - X_2^2 - \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}}\right)^{-1} \quad (33)$$

One can think of a zero-point as a particular combiner output power level at which the combiner happens to operate as an exact inverse of its corresponding resistance compression network. In other words, at a particular zero-point, all driving PAs see a purely conductive loading impedance of $1/R_o$, where $R_o$ is such that when compressed by the combiner's corresponding RCN, the RCN's input resistance is equivalent to the combiner's load.

To understand this better, consider the combiner example discussed above. At each of the combiner's four zero-points all four PAs are equally loaded with a purely conductive load of $1/R_o$. The value of $R_o$ is such that when compressed by the combiner's corresponding RCN of Fig. 2-3, it will result in an RCN input resistance $R_{in,2}$ equivalent to the combiner's load $R_L$. One would usually design the combiner so that $R_L = R_{in,2,med}$. Then, as can be seen from Fig. 2-3, there are exactly four possible $R_o$ values (12.2)-(12.5) at which $R_{in,2} = R_{in,2,med} = R_L$ (marked with a dot in Fig. 2-3), and hence, there are four zero-points in the combiner's admittance characteristic. Equations (30)-(33) are readily obtainable from (12.2)-(12.5) by replacing $R_{in,2,med}$ with $R_L$.

It can be shown that, in general, a $2^N$-way combiner will have $2^N$ zero-points. As Appendix B demonstrates for, an eight-way combiner, for example, has eight zero-points spread over a wider power range compared to the four-way combiner.

### 2.5.2. Optimal-Susceptance (OS) Outphasing Control

Another control methodology, optimal-susceptance (OS) outphasing control, is proposed which is characterized with the following two main advantages: (1) it minimizes the effective input susceptance seen by the PAs at each output power level, and (2) achieves even susceptive loading of the PAs (all PAs see approximately equivalent susceptive loading) over the desired operating output power range. Such an outphasing control methodology is advantageous in systems incorporating a power combiner driven by non-linear, switched-mode inverters/PAs, where susceptive variations in their loading is detrimental to the overall system efficiency.

For the four-way combiner discussed here (Fig. 2-3), the optimal susceptance control angle pair $[\theta; \phi]$ can be computed for a particular output power level $P_{out}$ by numerically minimizing the largest effective input susceptance $S_{max}$ seen by any of the PAs (at $P_{out}$) (34) subject to the constraint (35):

$$S_{max} = max\left\{\left|Im\left\{Y_{eff,A}\right\}\right|,\left|Im\left\{Y_{eff,B}\right\}\right|\right\} \tag{34}$$

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} sin^2(\phi)cos^2(\theta) \tag{35}$$

It can be shown that for the range of output power levels given by (36), which includes the power range between the combiner's outer two zero-points, the solutions of the preceding optimization problem (34), (35) reduce to a set of convenient analytical expressions for calculating the control angles (37):

$$\frac{P_{out,sat}}{2}\left(1-\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \le P_{out} \le \frac{P_{out,sat}}{2}\left(1+\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \tag{36}$$

$$\theta = cos^{-1}\left(\sqrt{\frac{4V_S^4 + P_{out}^2 X_1^2}{8P_{out}R_L V_S^2}}\right) \text{ and } \phi = tan^{-1}\left(\frac{P_{out}X_1}{2V_S^2}\right) \tag{37}$$

Fig. 2-7 shows a plot of the effective input conductance, susceptance and phase seen by each of the PAs driving the power combiner from the previous example ($R_L$ = 50Ω, $X_1$ = 36.69 Ω, and $X_2$ = 48.97 Ω). The zero-points occur at the same output power levels as in the case of the IRCN outphasing control and can be computed according to (30)-(33).

### 2.5.3. Optimal-Phase (OP) Outphasing Control

Third control methodology, optimal-phase outphasing control, is proposed which is characterized with its two main advantages: (1) it minimizes the effective input admittance phase seen by the PAs at each power level, and (2) ensures that each PA sees the same phase (in terms of absolute value) of the loading admittance. This outphasing control method may be preferred in a combining system where the combiner is driven by a set of linear amplifiers, such as class A, class B, or class AB.

For the 4-way combiner addressed here (see Fig. 2-5), the optimal susceptance control angle pair [θ; ϕ] can be computed for a particular output power level $P_{out}$ by numerically minimizing the largest effective input admittance phase $\varphi_{max}$ seen by the PAs (at $P_{out}$) (38) subject to the constraint (39):

$$\varphi_{max} = max\left\{tan^{-1}\left\{\left|\frac{Im\left\{Y_{eff,A}\right\}}{Re\left\{Y_{eff,A}\right\}}\right|\right\}, tan^{-1}\left\{\left|\frac{Im\left\{Y_{eff,B}\right\}}{Re\left\{Y_{eff,B}\right\}}\right|\right\}\right\} \tag{38}$$

$$P_{out} = \frac{8R_L V_S^2}{X_1^2} sin^2(\phi)cos^2(\theta) \tag{39}$$

It can be shown that for the range of output power levels given by (40), which includes the main operating range of practical interest, the solutions of the preceding optimization problem (38), (39) reduce to a non-linear system of equations (41) which can be solved for [θ; ϕ] by employing conventional numerical methods.

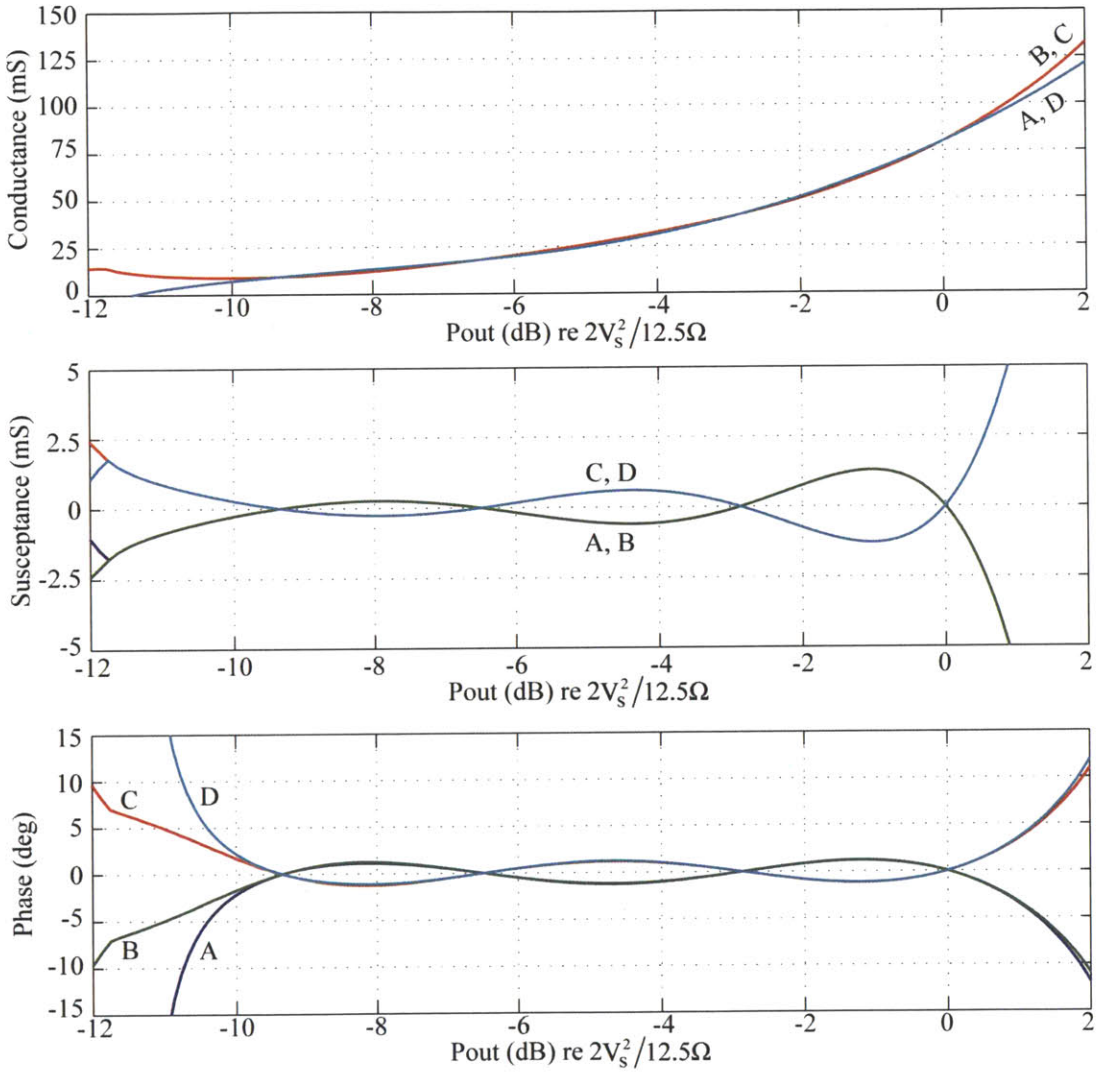



Fig. 2-7: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way combiner of Fig. 2-5 with $R_L = 50\ \Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$ as a result of OS outphasing control.

$$\frac{P_{out,sat}}{2}\left(1-\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \le P_{out} \le \frac{P_{out,sat}}{2}\left(1+\sqrt{1-\frac{X_1^2}{4R_L^2}}\right) \tag{40}$$

$$\frac{P_{out}X_1^2}{8R_L V_S^2} = sin^2(\phi)cos^2(\theta) \tag{41}$$

$$sin(2\phi) = \frac{2\gamma cos^2(\theta)}{\beta^2 + 4\gamma^2 cos^2(\theta) - 2\beta\gamma sin(2\theta)}$$

As an example, Fig. 2-8 shows a plot of the effective input conductance, susceptance and phase seen by each of the PAs driving the previously considered combiner from Fig. 2-5 ($R_L = 50\Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$).

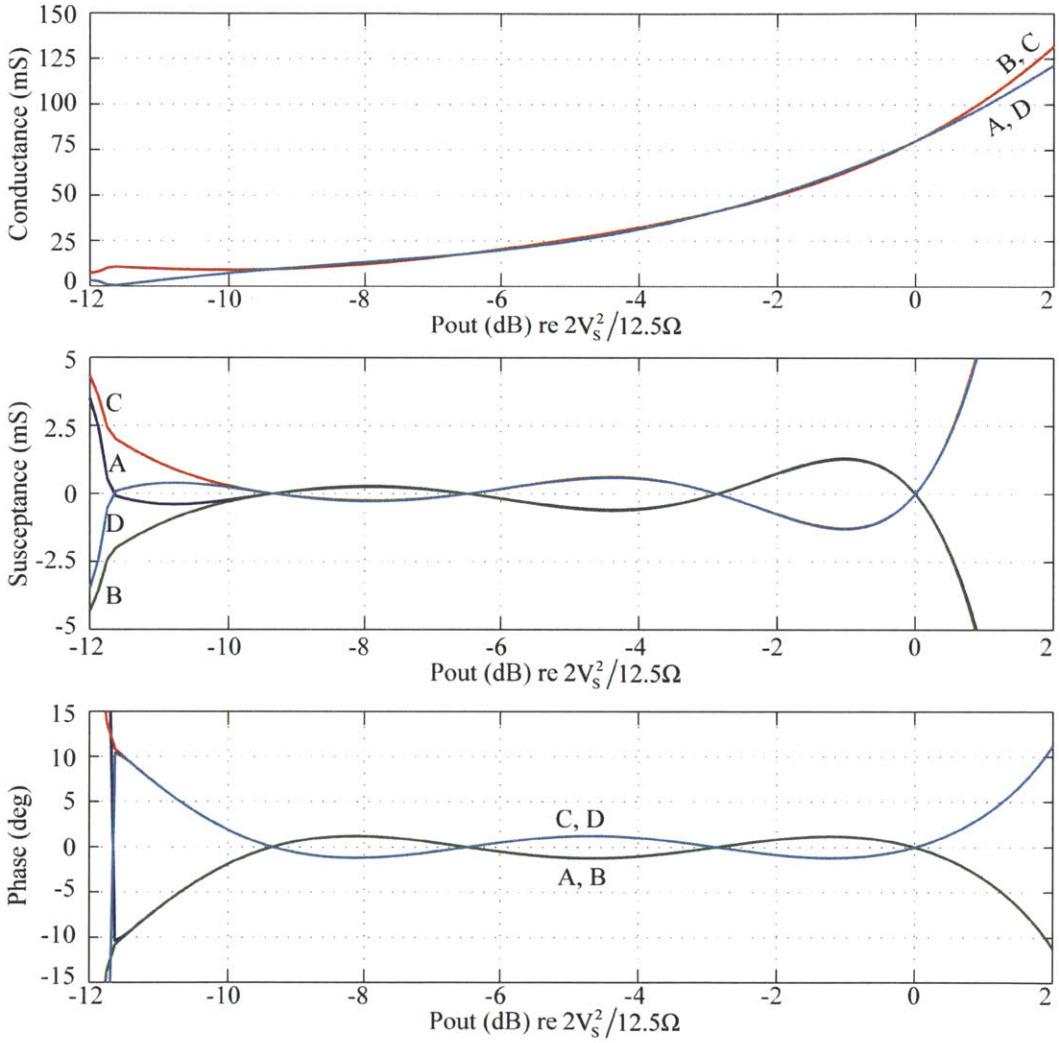



Fig. 2-8: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way combiner of Fig. 2-5 with $R_L = 50\ \Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$ as a result of OP outphasing control.

### 2.5.4. Comparison of Outphasing Control Methods

All of the above methodologies can be adopted for the outphasing control of a general N-way power combiner. Moreover, one could switch methodologies based on operation over different power ranges or for different operating conditions if desired. Nevertheless, to compare the relative performance of each

control method, consider as an example the power combiner of Fig. 2-5 with $R_L = 50\Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$. Fig. 1-5 shows the appropriate outphasing control angles $\theta$ and $\phi$ for each of the above control methods over a 20 dB output power range.

It can be clearly seen from Fig. 2-9 that the optimal-phase and optimal-susceptance control angles are almost entirely identical over a significant portion of the output power operating range. Thus by choosing the control angles to minimize the effective input admittance phase seen by the PAs, for all practical purposes, one effectively minimizes the susceptive components as well, and vice versa. Fig. 2-10 further demonstrates this observation by examining the worst-case input admittance phase and susceptance (absolute value) seen by the PAs for a particular output power level in the operating region of interest for the above 4-way power combiner example.

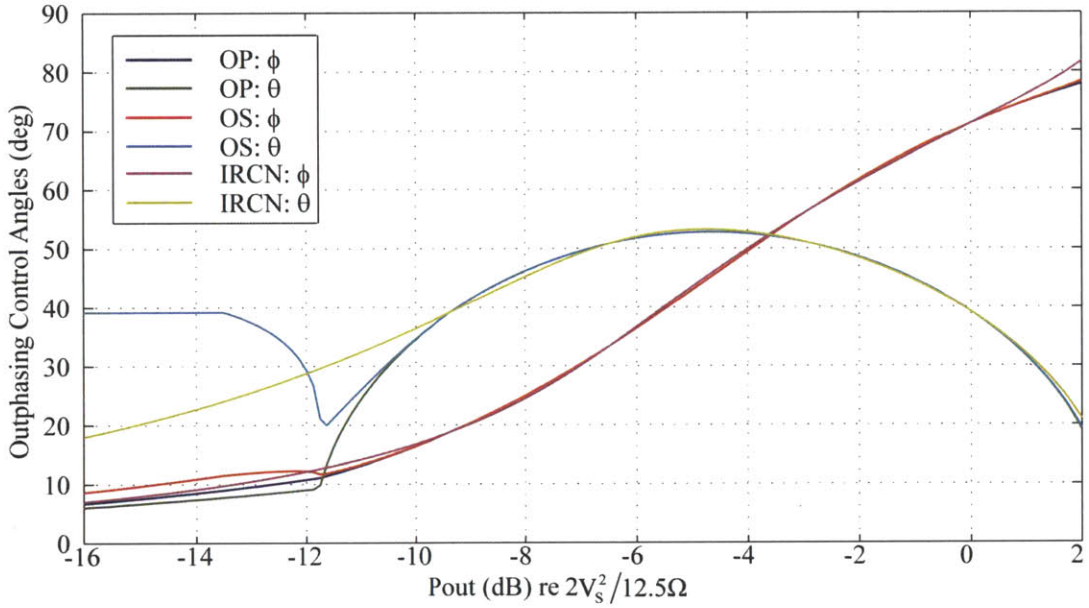



Fig. 2-9 Outphasing control angles $\theta$ and $\phi$ for the Optimal Phase (OP), Optimal Susceptance (OS), Inverse RCN (IRCN) control methods for the four-way combiner of Fig. 2-5 with $R_L = 50\ \Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$.

Furthermore, it is obvious from Fig. 2-10 that both control methods optimal-susceptance, and optimal-phase result in approximately equivalent phase and susceptance characteristics over the main operating power range with over four times improvement compared to the IRCN control method. For this example, the IRCN control method yields less than 5 degrees of admittance phase (absolute value) over more than a factor of ten in output power modulation, while the optimal-phase and optimal-susceptance methods result in a peak admittance phase of approximately a degree (over the 10 dB operating range).

Here it is important to note that the combiner effective input admittance characteristic (and hence the loading of the PAs) could very sensitive to the outphasing angles $\theta$ and $\phi$. For a particular output power level, the values of $\theta$ and $\phi$ can vary by a fraction of a degree from one control method to another. Demanding such an accurate outphasing control in a real system could be a challenging task. And although, one may not be able to guarantee a true OP, OS, or IRCN-control of the combiner in practice, modulation

of the output power over a very wide range is still possible at the cost of slightly higher susceptive variations in the PA loading. Nevertheless, it is important to present the OP, OS and IRCN control methods as a guideline for outphasing control and an indication of the optimal admittance characteristics that can be achieved for a particular combiner implementation. Appendix C (combiner4_outphasing_control.m) provides a MATLAB script capable of computing the OP, OS, and IRCN outphasing control angles for an arbitrary four-way combiner.

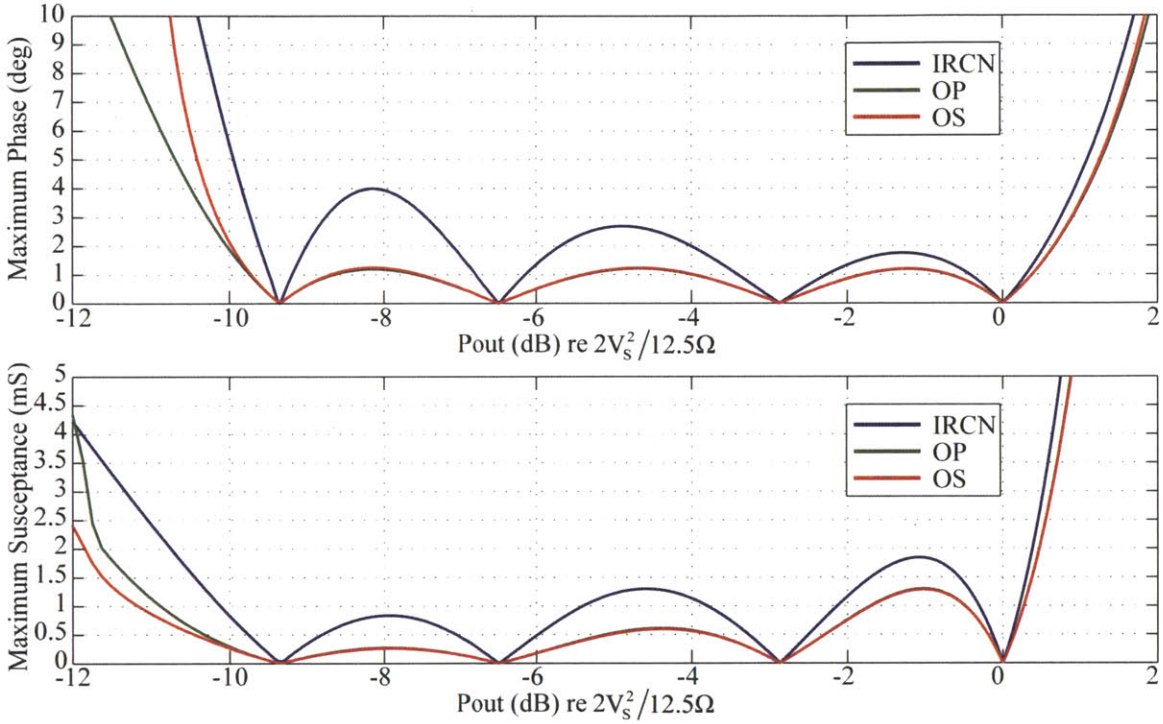



Fig. 2-10: Worst-case effective input admittance phase and susceptance seen by the PAs driving the four-way combiner of Fig. 2-5 with $R_L = 50\ \Omega$, $X_1 = 36.69\ \Omega$, and $X_2 = 48.97\ \Omega$ as a result of the optimal-phase (OP), optimal-susceptance (OS) and inverse RCN (IRCN) outphasing control methods.

## 2.6. Combiner Design Methodology

The previous subsection presented various outphasing control methodologies to control the output power of the proposed combiner. These control methodologies are based on the assumption that the combiner reactances were selected appropriately, i.e. the combiner was designed to operate over a particular output power range. This subsection details the design methodology and the process for selecting the combiner reactances ($X_1$ and $X_2$ in the case of the four-way combiner of Fig. 2-5).

Thinking of the proposed combiner architecture as an approximate inverse of the earlier-presented resistance compression networks, one would expect a similar procedure for selecting the combiner reactances, which are also equivalent to the reactances in the corresponding compression network. For example, consider the four-way combiner of Fig. 2-5 and its corresponding RCN of Fig. 2-3. The source $V_L$ driving the RCN (Fig. 2-3) sees an effective resistive loading $R_{in,2}$ which varies (with median $R_{in,2,med}$) as

the $R_o$ resistances vary. When the described time-reversal dualities are applied to the RCN (negating the sign of all reactances), the $V_L$ source effectively behaves as the combiner load resistance $R_L$, and the $R_o$ resistances behave as the PAs driving the combiner (see Fig. 2-5). If $R_L$ was to vary similarly to $R_{in,2}$, then the combiner would behave as an exact inverse of the RCN, and the PAs would see an entirely resistive load of $R_o$ over the entire operating range. However, in practical combining applications, the load $R_L$ is usually fixed. It is this mismatch between $R_L$ and $R_{in,2}$ that ultimately results in small, but non-zero susceptive components of the PAs' loading. To minimize the mismatch between $R_L$ and $R_{in,2}$, one can choose $R_L$ to be equivalent to the median of $R_{in,2}$, i.e. $R_L = R_{in,2,med}$. Thus, the combiner reactances can now be calculated by employing the same design equations as for the compression network. This approach for selecting the combiner reactances is valid for any $2^N$-way combiner, and is further detailed in Appendix B.

In the case of the four-way combiner of Fig. 2-5, $X_1$ and $X_2$ can be computed by reusing equations (6), (10), (11), and setting $R_{in,2} = R_L$. In other words, to design the combiner for a particular load $R_L$, select the reactances $X_1$ and $X_2$ according to (42) and (43):

$$X_2 = \frac{2R_L}{k+1} \tag{42}$$

$$X_1 = \frac{X_2}{k+\sqrt{k^2-1}} \tag{43}$$

One can think of k as a design parameter uniquely determining the behavior and performance of the power combiner; its value directly controls the width of the output power operating range and the spread of the zero-points. Fig. 2-11 plots the maximum absolute value of the loading admittance phase seen among the PAs at a particular power level for various values of k.

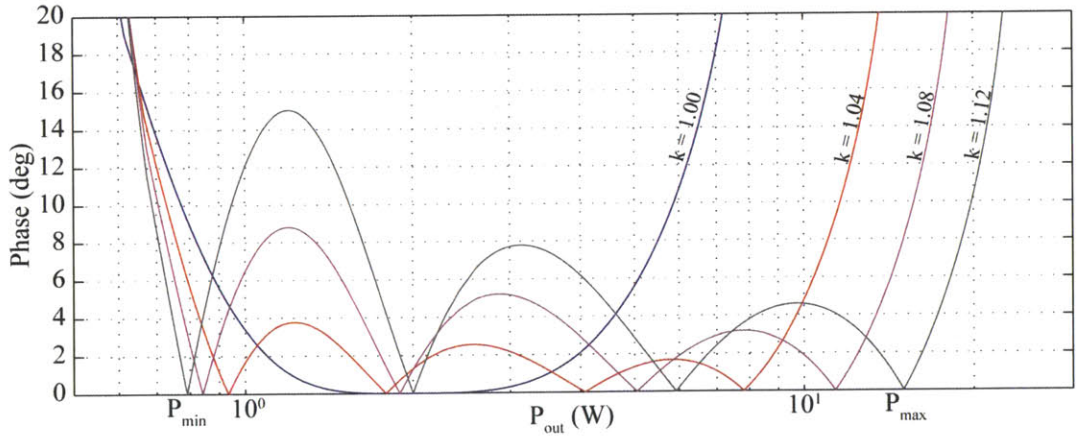



Fig. 2-11: Absolute value of the maximum effective input admittance phase seen at the input ports of a four-way power combiner versus the output power level for various k-values. The plot is normalized to $V_S$ = 1 V and $R_L$ = 1 Ω; denormalize for a particular $V_S$ and $R_L$ by scaling the $P_{out}$ axis by $V_S^2/R_L$.

Although the plot is generated assuming an IRCN outphasing control, the observations discussed below are valid for any of the proposed outphasing controls. The power axis is normalized to $R_L = 1\ \Omega$ and $V_S = 1V$. To denormalize for a particular value of $R_L$ and $V_S$, simply scale the axis by $V_S^2/R_L$. As can be seen from Fig. 2-11, a larger k-value results in a wider operating range at the cost of larger susceptive (and phase) variations of the combiner's input admittances. On the other hand, smaller k-values reduce susceptive variations (and phase), but in-turn narrow the operating range of the combiner. It is important to clarify here that by talking about the operating range of the combiner, one refers to the power range between the outer two zero-points of the combiner's admittance characteristic. For example, in Fig. 2-11, the operating range for k = 1.12 will be $[P_{min}, P_{max}]$. It is over this power range that the variations of the combiner's input admittances are minimized. Of course, by selecting the appropriate outphasing control angles, one could make the combiner to operate outside of this power range (beyond the outer zero-points), although in this case, the PAs would see significant susceptive loading components which could adversely impact the overall system efficiency. Nevertheless, if the combiner is occasionally required to operate beyond the outer zero-points, this could be achieved by appropriately adjusting the PA drive amplitudes instead of phase-shifting them.

The design chart of Fig. 2-12 has been generated (see Appendix C, combiner4_design_curves.m for MATLAB script) to provide a convenient tool for selecting the appropriate k-value for a particular combiner output power range ratio (PRR) for the four-way combiner of Fig. 2-5. PRR is the ratio of the power levels at which the outer two zero-points occur (expressed in dB). The value of k is found by tracing horizontally from the specified power ratio to the Power Ratio Curve of interest, and tracing vertically to find k. The respective peak (worst-case) admittance phase that results from operation over this power range can be obtained by tracing the k-value of choice vertically to the appropriate Phase Curve (depending on whether OP, OS, or IRCN outphasing control is used) and then horizontally (right) to the corresponding worst-case admittance phase. Similar design chart (Fig. 2-13) is provided which shows the corresponding peak susceptance for a particular PRR (normalized to $1/R_L$) under OS, OP and IRCN outphasing control. Moreover, Fig. 2-14 depicts the actual power levels corresponding to each of the four zero-points $P_{out,zp1}$ - $P_{out,zp4}$ in the combiner's admittance characteristic given by (30)-(33). Note that the power axis is normalized to $R_L = 1\ \Omega$ and $V_S = 1V$. To denormalize for a particular value of $R_L$ and $V_S$, simply scale the axis by $V_S^2/R_L$. It is easily seen from Fig. 2-14 that selecting a larger k-value results in spreading the zero-points further apart, and hence increasing the combiner's operating range.

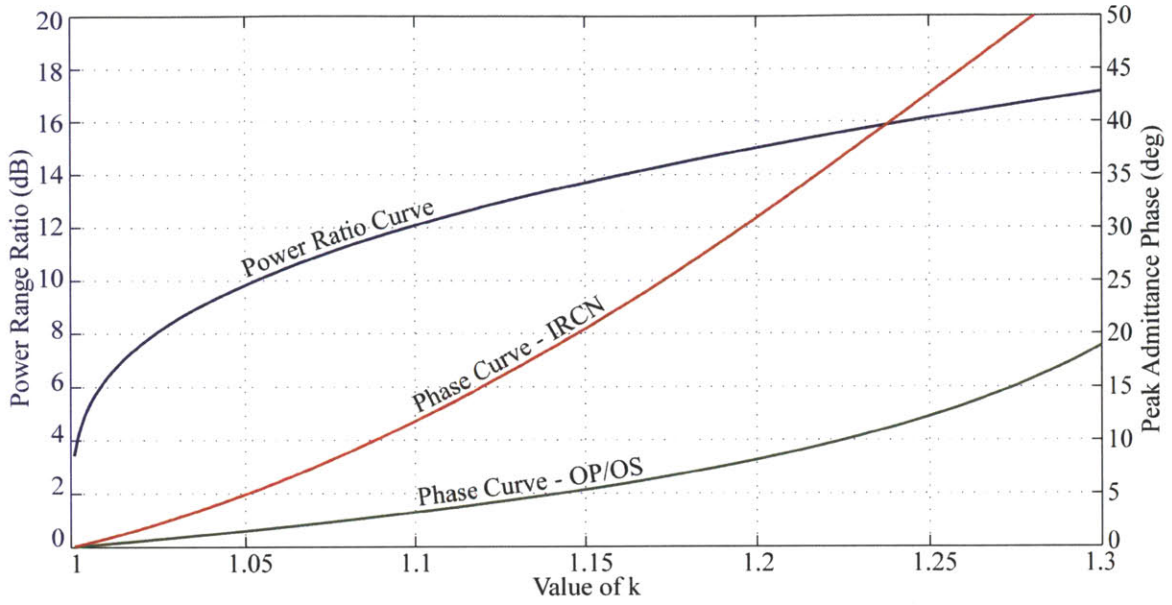



Fig. 2-12: Four-way combiner design curve: trace-out the specified power range ratio to the Power Ratio Curve to determine the appropriate design value for k. The Phase Curves give the corresponding peak effective input admittance phase that a PA can see at the inputs ports of the combiner over the specified operating range for IRCN, or OP/OS outphasing control respectively.

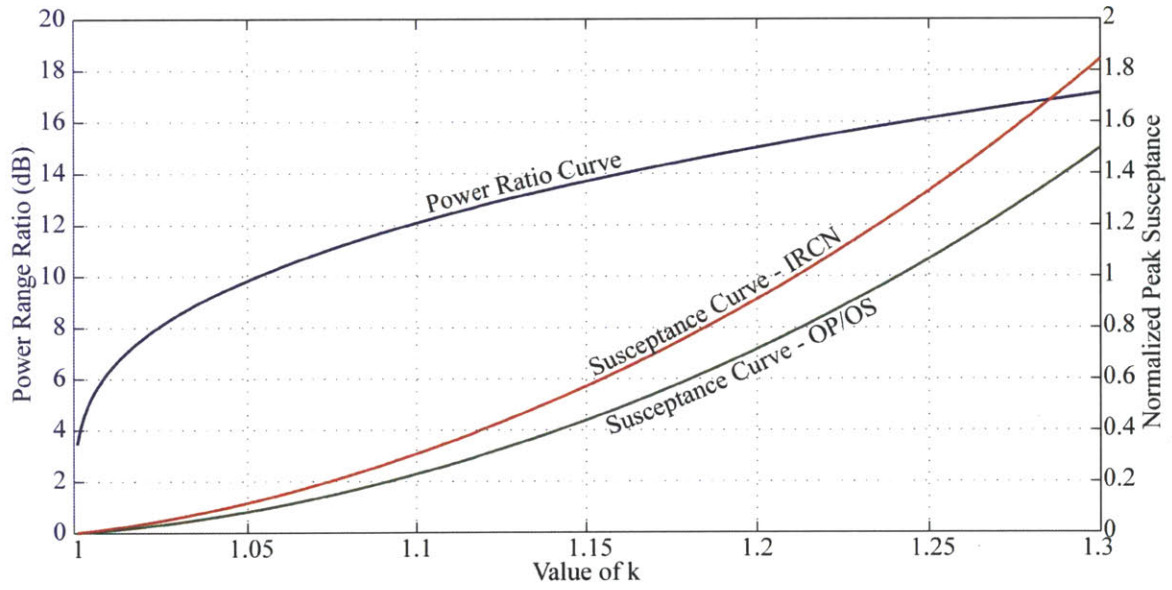



Fig. 2-13: Four-way combiner design curve: trace-out the specified power range ratio to the Power Ratio Curve to determine the appropriate design value for k. The Susceptance Curves give the corresponding peak effective input susceptance that a PA can see at the inputs ports of the combiner over the specified operating range for IRCN, or OP/OS outphasing control respectively. The susceptance axis is normalized to a combiner load $R_L = 1\ \Omega$; to denormalize, multiply axis by $1/R_L$.

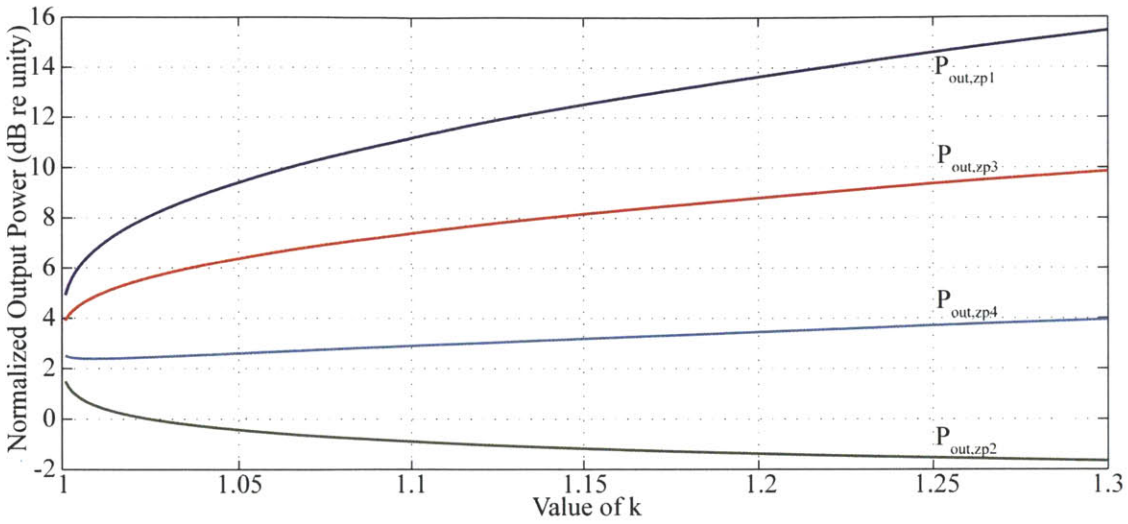



Fig. 2-14: The output power level corresponding to each of the zero-points $P_{out,zp1}$ - $P_{out,zp4}$ versus the k-value for the four-way combiner. Output power is normalized to $V_S = 1$ V and $R_L = 1\ \Omega$; denormalize for a particular $V_S$ and $R_L$ by scaling the axis by $V_S^2/R_L$.

## 2.7. Combiner Sensitivity to Loading Variations

Although the combiner is ideally designed to deliver power to a fixed and well-known load impedance (at the operating frequency), in reality, its value may vary by a certain amount (both resistively and reactively). Consequently, this could result in significant variation to the PA loading characteristics from the ones already described above. This subsection presents an intuitive approach for understanding the effect of such loading impedance variations on the combiner's input port characteristics.

Consider the four-way combiner of Fig. 2-5 designed to operate with a loading impedance $Z_L = R_L$. Now suppose that this impedance changes by a resistive increment $\Delta R_L$ and a reactive increment $\Delta X_L$, i.e. $Z_L = (R_L + \Delta R_L) + j\Delta X_L$. To determine the effect of this load variation on the combiner's effective input admittances, one can first determine the resultant combiner input-port current increments $\Delta I_A$ - $\Delta I_D$ (sourced by the PAs). Since the driving voltage waveforms at the combiner input terminals are maintained unchanged both in phase and amplitude by the PAs (treating the PAs as ideal voltage sources), the resultant effective input admittances can then be easily determined.

One possible way for calculating $\Delta I_A$ through $\Delta I_D$ is by applying the alteration theorem [56]: the PAs are short-circuited, and the modified load $Z_L = (R_L + \Delta R_L) + j\Delta X_L$ is replaced by a voltage source $V_T = I_L(\Delta R_L + j\Delta X_L)$, where $I_L$ is the *original* load current (when $Z_L = R_L$). The modified circuit is illustrated in Fig. 2-15. By employing conventional linear circuit analysis techniques, it is readily shown that the incremental currents are given by (50). This is easy to see since the effective parallel impedance of reactive branch pairs A/B, and C/D is infinite, and so the voltage at nodes $N_1$ and $N_2$ is $V_{N1} = V_{N2} = V_T = I_L(\Delta R_L + j\Delta X_L)$. Moreover, $I_L$ can be further expressed in terms of the output power $P_{out}$ delivered to the original load

$R_L$ ($\Delta R_L = \Delta X_L = 0$). The sign in (50) is selected depending on the nature of the $X_1$ reactive branch: (+) for an inductive branch and (-) for a capacitive branch.

$$\Delta I_{A-D} = \pm j\frac{I_L(\Delta R_L + j\Delta X_L)}{X_1} = \pm j\frac{(\Delta R_L + j\Delta X_L)}{X_1}\sqrt{\frac{2P_{out}}{R_L}} = \pm\sqrt{\frac{2P_{out}}{R_L}}\frac{(-\Delta X_L + j\Delta R_L)}{X_1} \qquad (50)$$

A current increment $\Delta I_A$ - $\Delta I_D$ can introduce additional phase $\varphi$ between a PA's output current and voltage waveforms, and consequently alter its effective loading. Fig. 2-16 illustrates this in the case of the PA driving the capacitive branch A (Fig. 2-5). Originally (when $\Delta R_L = \Delta X_L = 0$), the PA's output voltage $V_A$ and current $I_A$ are approximately in phase (a reasonable approximation for narrow operating power ranges and over much of the operating range of interest). A variation in the combiner's load produces a current increment $\Delta I_A = \Delta I_{A,re} + j\Delta I_{A,im}$, which adds to the original PA output current $I_A$ and results in an effective input admittance phase $\varphi$.

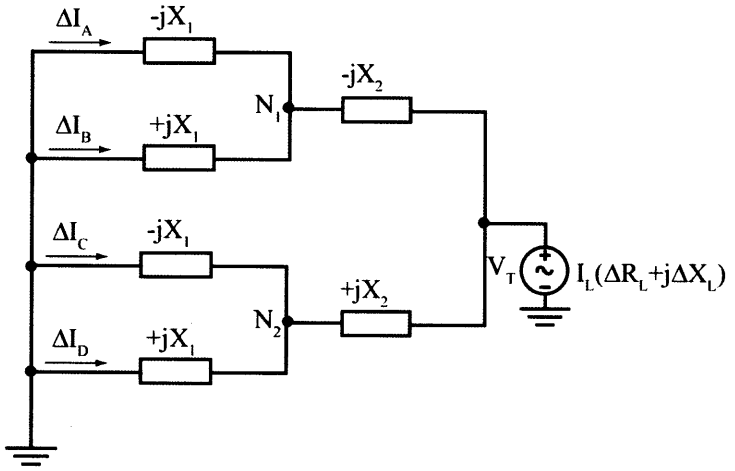



Fig. 2-15: Network utilized for analyzing the incremental change of sourced input currents by the power amplifiers (Fig. 2-5) for a given incremental resistive/reactive change in load impedance $R_L$ by employing the Alteration Theorem [56]. $I_L$ is the load current in Fig. 2-5 when $\Delta R_L = \Delta X_L = 0$.

As an example, consider Fig. 2-17 illustrating the effect of 2.5% and 5% resistive variations (top) and reactive variations (bottom) of the nominal 50 Ω, purely-resistive combiner load on the input admittance phase characteristic of the four-way combiner of Fig. 2-5 with $X_1$ = 36.69 Ω, and $X_2$ = 48.97 Ω (designed to operate over a 10 dB power back-off range). As can be seen, even small variations of the combiner loading may have appreciable effect on the effective PA loading, although even for +/- 5% variations the PA loading still remains mostly resistive.

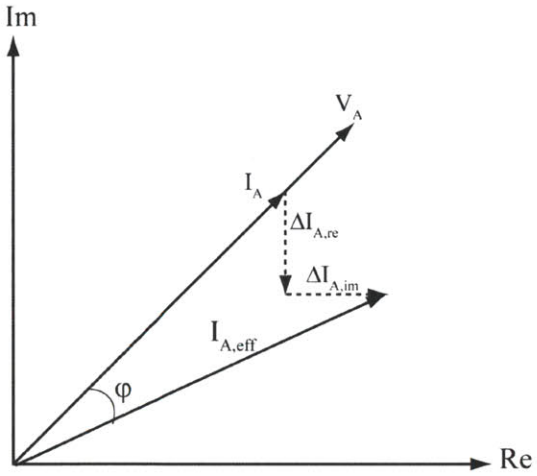



Fig. 2-16: Phasor diagram illustrating the effect of combiner load variation on its effective input admittance. The input terminal current increments $\Delta I_{A,re}$ and $\Delta I_{A,im}$ resulting from deviation of the combiner's load from its nominal value introduce additional input admittance phase.

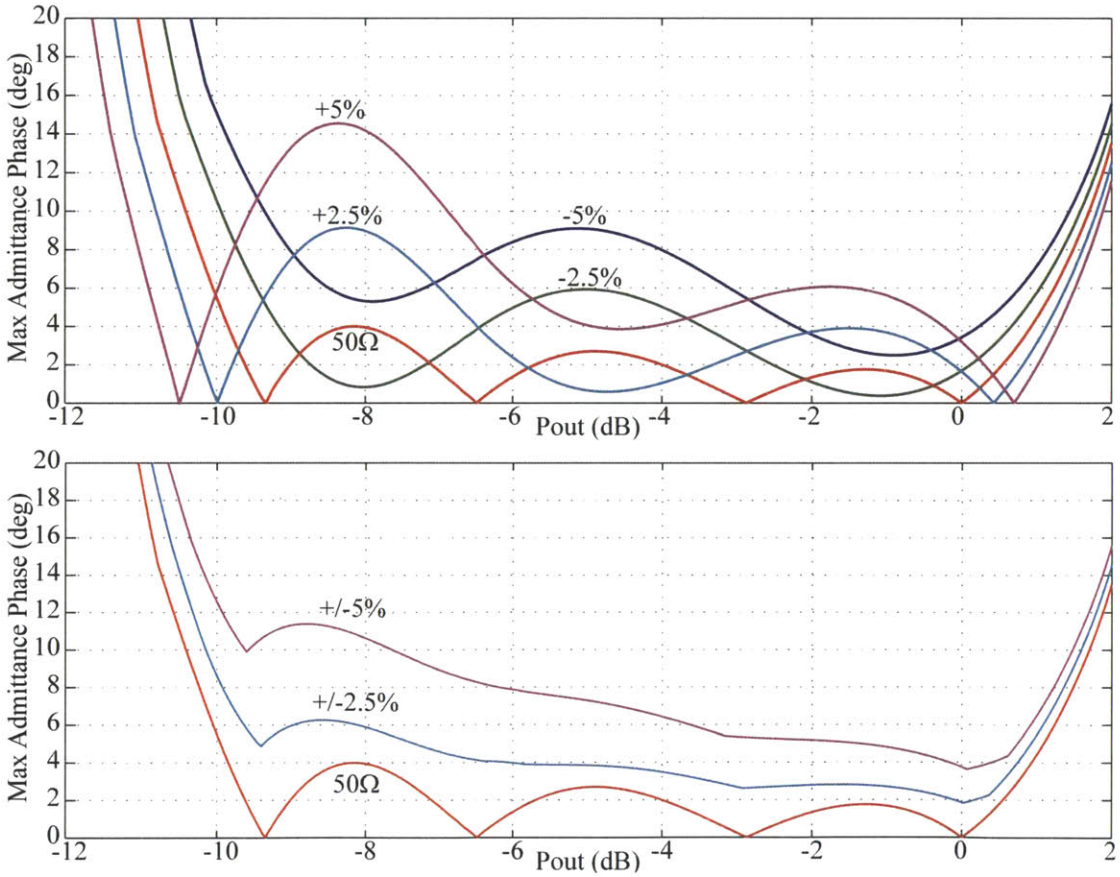



Fig. 2-17: Maximum admittance phase (absolute value) seen among the PAs driving the four-way combiner of Fig. 2-5 ($R_L$ = 50 Ω, $X_1$ = 36.69 Ω, and $X_2$ = 48.97 Ω) versus output power back-off as a result of 2.5% and 5% purely-resistive (top plot) and purely-reactive (bottom plot) variations of the 50 Ω nominal combiner load.

## 2.8. Topological Variations

The discussion in the above subsections has so far focused only on the combiner implementation shown in Fig. 2-5. This combiner implementation may be thought of as including a binary tree of reactances having complementary reactances at each bifurcation in the tree. For a "Binary Tree" combiner implementation with M bifurcations, one has $N = 2^M$ inputs and 2N-2 reactive branches. As an example, Fig. 2-18 depicts such a "binary tree" implementation of an eight-way combiner (N=8). Nevertheless, various topological transformations may be applied to this basic "binary tree" realization to obtain other useful implementations of the combiner. Two such types of topological transformations are discussed here: (1) T-Δ network transformation (also known as the Y-Δ or star-triangle transformation), and (2) topological duality transformation. These transformations are exemplified here to enumerate other possible topological implementations of the four-way combiner; similar techniques can be used to synthesize higher-order combiners. Although the input-port and output-port characteristics, as will be demonstrated below, remain largely unaffected under these transformations, depending on the application of the combiner and component values that result, one implementation may be preferred over another.

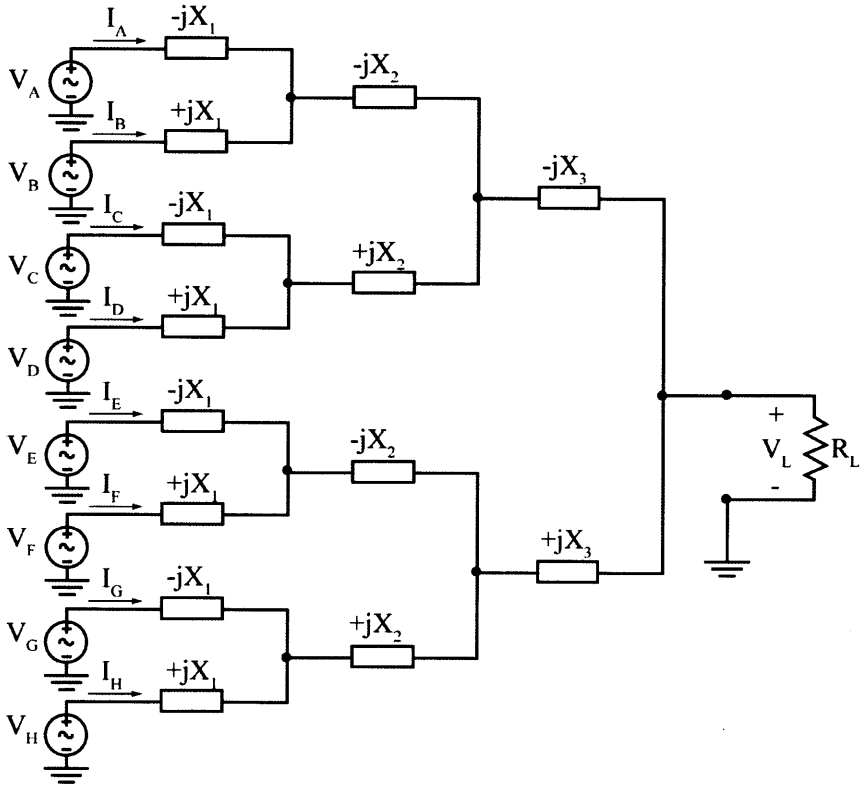
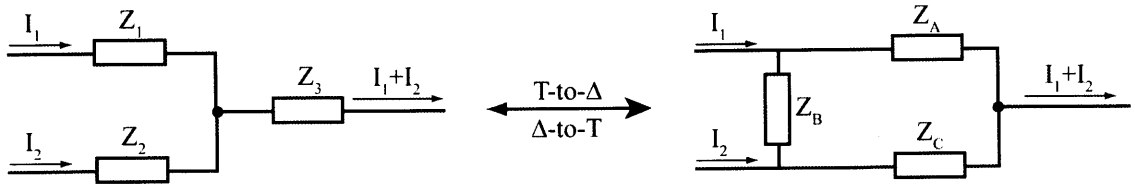



Fig. 2-18: A "binary tree" implementation of an 8-way power combiner.

### 2.8.1. T-Δ Network Transformations

The general T-Δ network transformation of a three-terminal network is illustrated in Fig. 2-19.




$$Z_1 = \frac{Z_A Z_B}{Z_A + Z_B + Z_C} \qquad Z_A = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_2}$$

$$Z_2 = \frac{Z_B Z_C}{Z_A + Z_B + Z_C} \qquad Z_B = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_3}$$

$$Z_3 = \frac{Z_A Z_C}{Z_A + Z_B + Z_C} \qquad Z_C = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_1}$$

Fig. 2-19: T-Δ general network transformation

An important characteristic of the transformation is that it does not affect the transformed network's interface with other networks connected to its terminals. In other words, the current-voltage relationship at each terminal of the transformed network is preserved under the transformation. Fig. 2-20 depicts the same transformation applied to top T-network of the power combiner in Fig. 2-5.

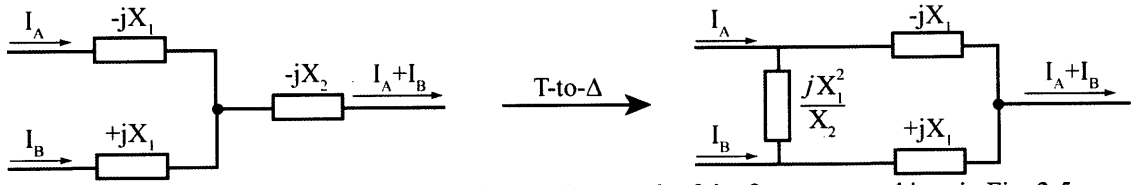



Fig. 2-20: T-to-Δ transformation applied to the top T-network of the four-way combiner in Fig. 2-5.

Fig. 2-21 illustrates the four-way combiner implementations that can result from applying the T-Δ transformation to the various T-networks found in the basic four-way combiner of Fig. 2-5 (repeated in Fig. 2-21(A) for convenience). Although unnecessary, it is convenient to think of the basic combiner in Fig. 2-21(A) as the starting point for all the T-Δ transformations. For this reason, the reactance magnitudes in all the implementation variants of Fig. 2-21(B)-(E) are given in terms of the reactance magnitudes of the basic combiner. The suggested reactance magnitude values for a particular implementation ensure that its input-port and output-port characteristics are identical to those of the basic combiner, i.e. as far as the PAs and the load (transformed in the case of Fig. 2-21(B)) are concerned, the behavior of the transformed combiner for any outphasing control method will be equivalent to that of the basic combiner for the same outphasing control strategy and respective load. It should be noted that the same transformations can be applied to the combiner and load networks in other power combiner implementations, including those of higher order N.

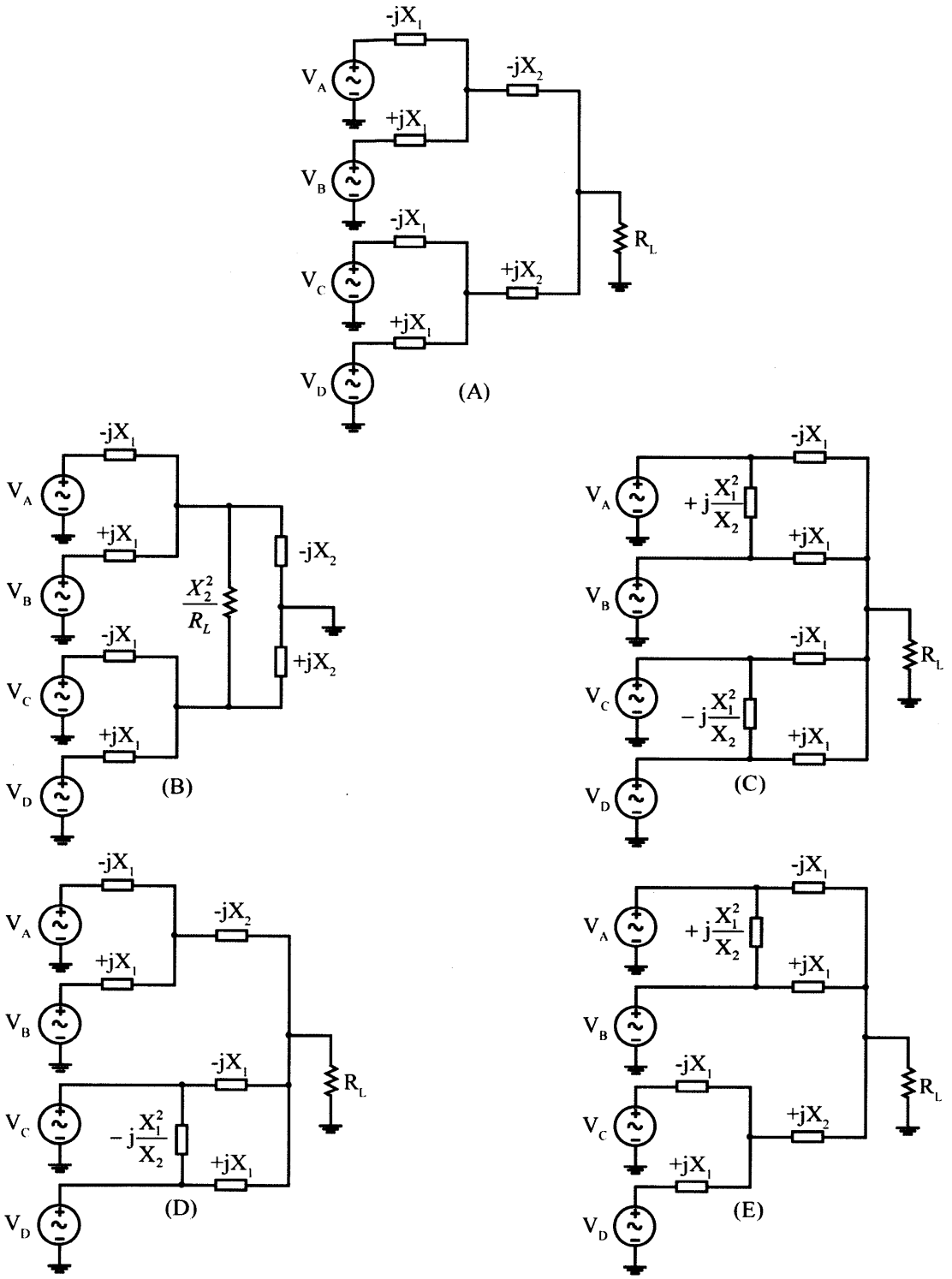



Fig. 2-21: Four possible topological variations (B)-(E) of the basic four-way combiner (A) as result of T-Δ transformations on portions of the network and load.

### 2.8.2. Network Duality

Fig. 2-22 shows the topology of the corresponding topological duals of each of the networks including four-way combiner implementations of Fig. 2-21.

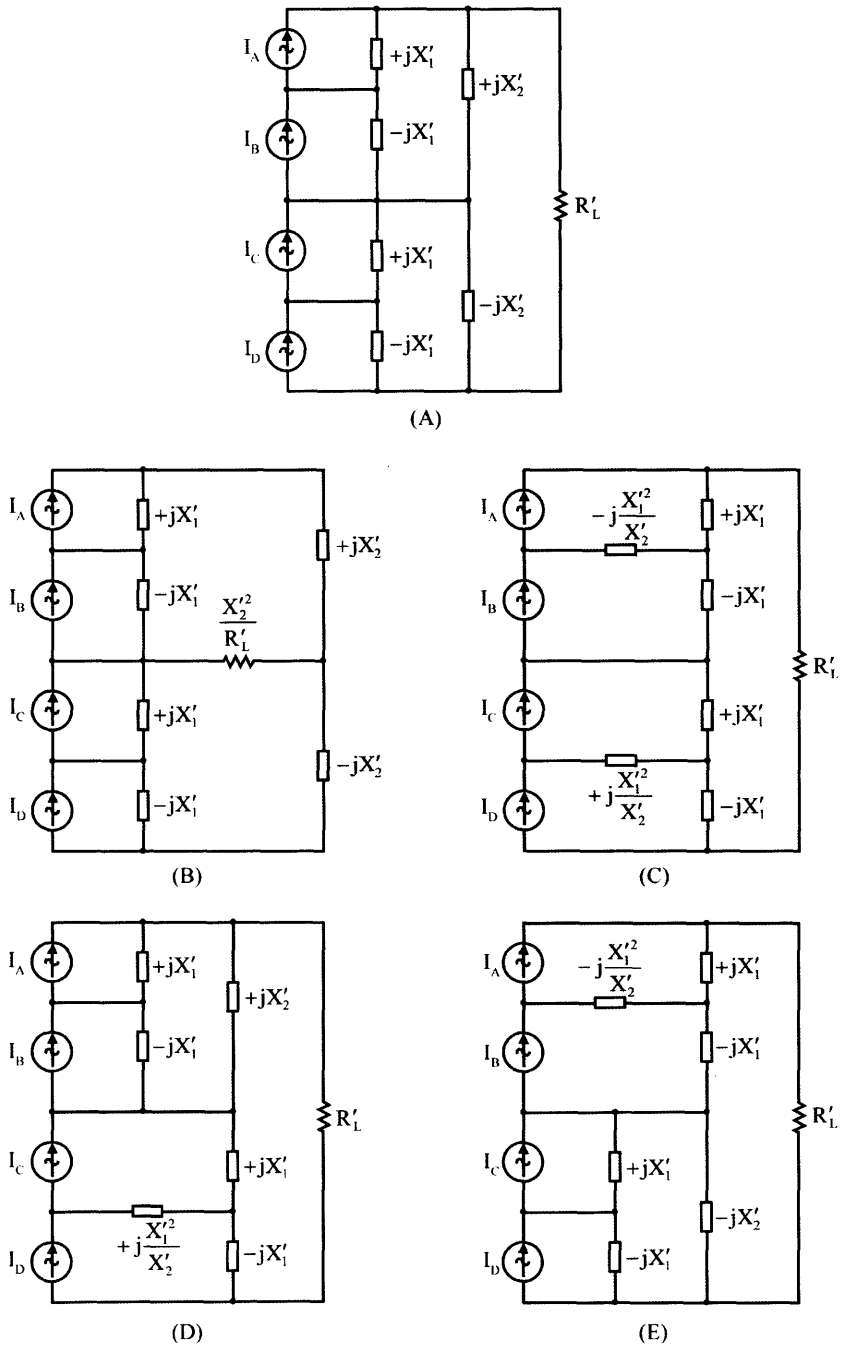



Fig. 2-22: Circuits corresponding to the topological duals of the circuits in Fig. 2-21. These circuits illustrate additional four-way combiner implementations. The power amplifiers are modeled as current sources in this representation (illustrating the input ports of the combiners). Magnitude and phase of the current sources is respectively equivalent to the magnitude and phase of the voltage sources in Fig. 2-21.

Specific component values may be found for the dual network as is well known [61]. As a result of this transformation, the PAs (approximated by voltage sources $V_A$-$V_D$ in Fig. 2-21) are now modeled respectively by currents sources $I_A$-$I_D$ having equivalent magnitude and phase relationship as the voltage sources of Fig. 2-21, though it is recognized that this is for modeling purposes, and to show the connection ports of the power amplifiers - the power amplifiers needn't act as ideal voltage or current sources.

Further, it is of significant importance to note that for any particular outphasing control method, the input admittance versus output power characteristic of the Fig. 2-21 permutations is equivalent to the input *impedance* versus output power characteristic of their respective duals. Conveniently, the relationship between the output power delivered to the load and the outphasing control methodology is unaffected by the topological duality transformation. Thus, all of the presented outphasing control methods previously introduced are directly applicable to the implementation variants of Fig. 2-22, although, in this case, it will be more appropriate to refer to the optimal-susceptance control method as the optimal-reactance control method, in keeping with the effects of topological duality on interchanging voltages and currents and admittances and impedances. (Note that other methods exist for synthesizing the networks of Fig. 2-22, such as starting with other types of multi-level resistance compression networks.)

## 2.9. Combining Power Losses and Efficiency

A concern with any power combining system is the efficiency of the combiner itself. While ideally lossless, the parasitic resistances of actual passive components (inductors and capacitors) in the combiner may contribute a degree of loss which cannot be neglected in some cases [60]. This section explores the impact of such combiner component power losses on the overall combining efficiency. Moreover, the effect of the various topological combiner implementations on its combining efficiency is also addressed. Note however that only power losses owing to the combiner components are treated here; driving-related losses that may accrue in the power amplifiers themselves (e.g., due to variations in effective impedances at the input ports of the power combiner) are not considered. The discussion here is limited to the four-way combiner, although Appendix B extends it to the case of the eight-way combiner.

### 2.9.1. Quality-Factor Power Losses

Consider the "binary-tree" implementation of the four-way combiner of Fig. 2-5. Assume that each branch in the combiner network has a series resistance $R_S$ such that every branch has the same quality factor $Q = |X|/R_S$. It is recognized that in general, capacitors tend to have higher quality factors than inductors. However, in an actual combiner implementation, one usually would realize each of the reactive branches as a series combination of an inductor and a capacitor (see Chapter 3 for details). As a result, the effective quality factor of each combiner branch is dominated by that of the inductor, and so all branches have approximately equivalent Q-factors (assuming identical types of inductors are used for every branch).

To estimate the losses and efficiency degradation owing to these parasitic resistances, a method that has been previously employed in matching networks [56], [57] is adopted: the circuit currents are calculated assuming no loss (i.e., assuming $R_S = 0$); the losses and circuit efficiency are then calculated based on the losses induced by the calculated currents flowing through the parasitic resistances. This method relies on the assumption that branch currents are not significantly affected by the presence of small resistances [56], [57] and has been demonstrated to be sufficiently accurate in modeling Q-factor losses associated with the power-combiner discussed here [29]. Using the above method, it can be shown that the power loss in the combiner $P_{loss,av}$ can be calculated as per (44) [29]:

$$P_{loss,av} = \frac{1}{2Q}\vec{V}^H\left[Y^H W Y\right]\vec{V} \tag{44}$$

where V and Y are defined as in (16) and (17), both being dependant on the particular outphasing strategy employed, $^H$ is the Hermetian operator (conjugate transpose), and W is the loss matrix given in terms of the combiner reactances $X_1$ and $X_2$ (45).

$$W = \begin{bmatrix} |X_1|+|X_2| & |X_2| & 0 & 0 \\ |X_2| & |X_1|+|X_2| & 0 & 0 \\ 0 & 0 & |X_1|+|X_2| & |X_2| \\ 0 & 0 & |X_2| & |X_1|+|X_2| \end{bmatrix} \tag{45}$$

Moreover, the fractional loss FL = (1-efficiency) of the combiner can be similarly calculated as [29]:

$$FL = 1-\eta = \frac{1}{Q}\cdot\frac{\vec{V}^H\left[Y^H W Y\right]\vec{V}}{\vec{V}^H Y \vec{V}} \tag{46}$$

Thus, it is inversely proportional to the quality factor of the combiner branch reactances, and depends on the operating point. Figure 2-23 shows the fractional power losses for Q = 100 (an achievable value in practice for many applications) for the four-way combiner of Fig. 2-5 versus normalized output power as a percentage of the combiner's saturation output power level (25) for several operating power range ratios. Each fractional loss curve was obtained by evaluating (46) over the operating range of a power combiner designed for the corresponding power range ratio according to the methodology outlined in Section 2.6 (see Appendix C, combiner4_q_loss_v2.m for a MATLAB script). An IRCN outphasing control (see Section 2.5.1) was assumed in this case, although results do not differ significantly from one control law to another.

As Fig. 2-23 demonstrates, combiners designed to operate over wider operating ranges are associated with slightly higher combining losses. Nevertheless, the predicted losses even for a 16 dB combiner are less than 10% (a combining efficiency greater than 90%). Thus, one would expect that the overall efficiency of

a power combining system will be mainly dominated by the PA efficiency, rather than the actual combining losses.

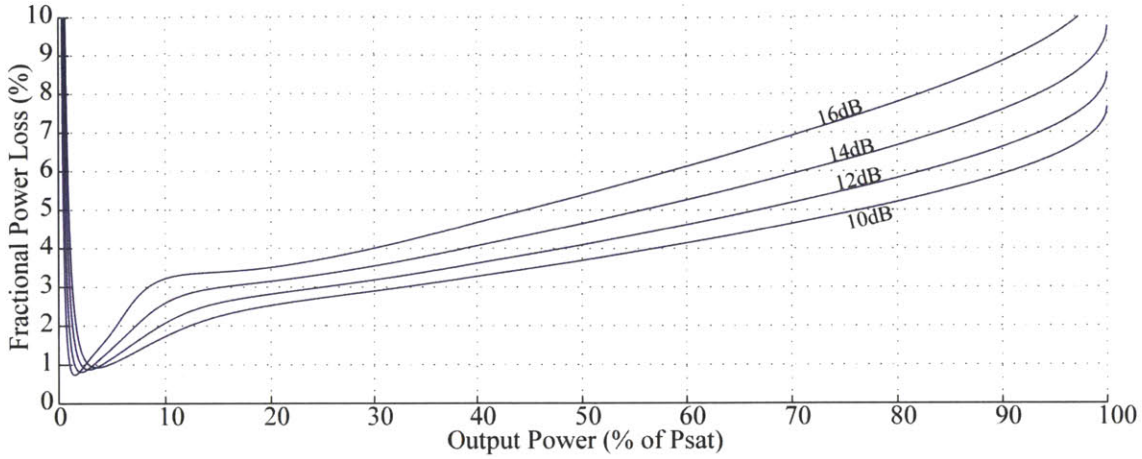



Fig. 2-23: Fractional four-way combiner power loss due to the finite Q-factor of its reactive branches versus output power for various operating range designs; a quality factor Q = 100 is assumed for all reactive branches.

### 2.9.2. Effect of Topological Transformations on Combiner Efficiency

As was presented earlier (see Section 2.8), various topological transformations can be performed on the basic "binary-tree" combiner implementation which can be classified in two main types: (1) the T-Δ transformation, and (2) the duality transformation. Although both transformation have no effect on the combiner's input/output-port characteristics (e.g. effective input admittances, output power control, outphasing, etc.), the T-Δ transformation affects to a certain degree the power combiner efficiency related to the finite Q-factor of its components. (It can be shown that the duality transform has no such effect on the efficiency of the power combiner for given quality-factors remaining constant, though practical components may have different achievable quality factors than yielded by the transformation.)

As can be seen from the general "binary-tree" combiner implementation, it consists entirely of cascaded T-networks; these can be thought as the fundamental building blocks of the overall network. Consider the T-Δ transformation of such a building block shown in Fig. 2-24. The corresponding Q-factor loss matrices $W_T$ and $W_\Delta$ for the T and Δ networks are respectively given by (47) and (48).

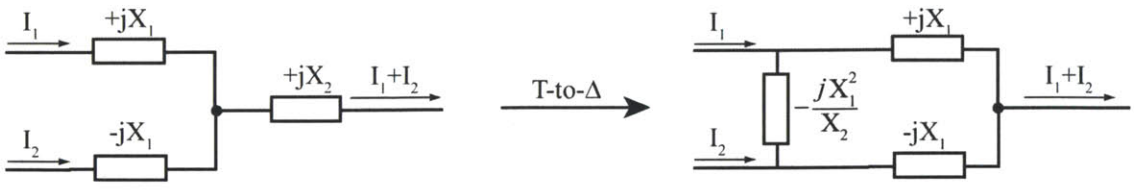



Fig. 2-24: T-to-Δ transformation applied to a T-network in the "binary-tree" combiner implementation.

$$W_T = \begin{bmatrix} |X_1|+|X_2| & |X_2| \\ |X_2| & |X_1|+|X_2| \end{bmatrix} \tag{47}$$

$$W_\Delta = \begin{bmatrix} X_2 + \frac{|X_2|^2}{X_1} + X_1\left(1+\frac{X_2}{X_1}\right)^2 & X_2 - X_2\left(1-\frac{X_2}{X_1}\right) + X_2\left(1+\frac{X_2}{X_1}\right) \\ X_2 - X_2\left(1-\frac{X_2}{X_1}\right) + X_2\left(1+\frac{X_2}{X_1}\right) & X_2 + \frac{|X_2|^2}{X_1} + X_1\left(1-\frac{X_2}{X_1}\right)^2 \end{bmatrix} \tag{48}$$

Since the terminal currents $I_1$ and $I_2$ are not affected by the transformation, and assuming the same quality factor Q for all inductive and capacitive components, it can be shown that the incremental power loss associated with the transformation is given by:

$$\Delta P_{loss} = P_{loss,\Delta} - P_{loss,T} = \frac{1}{Q}\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}^H (W_\Delta - W_T)\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{49}$$

where, $P_{loss,\Delta}$ and $P_{loss,T}$ are the power losses associated with the $\Delta$ and T networks of Fig. 2-24 respectively. The corresponding incremental fractional power loss can easily be computed by finding the ratio of (49) to the total delivered power to the power combiner. As can be seen from (47)-(49), the incremental loss for a given T-$\Delta$ transformation depends only on the operating point and the elements which are involved in the transformation. As a result, one can easily determine the effect of an arbitrary number of such T-$\Delta$ transformations on the various branches of the basic "binary-tree" combiner implementation by simply computing the incremental losses associated with each transformation and adding them to losses of the "binary-tree" implementation (also referred to as the T-implementation). By plotting the incremental losses for a given T-$\Delta$ transformations over the entire operating power range of a combiner, one obtains the so-called *incremental loss* curves. This approach is applicable to the general multi-way power combiner (see Appendix B for illustration in the case of the eight-way combiner).

Fig. 2-25 shows the T-implementation of a two-stage combiner along with outlined component groups over which a T-$\Delta$ transformation may be applied, and Fig. 2-26 illustrates the respective incremental loss curves. Note that if several possible transformations involve a common component, then only one of the transformations can be applied. For example, as can be seen from Fig. 2-25, a $\beta$-transformation can not be followed by an $\alpha$-transformation. However, performing two $\alpha$-transformations simultaneously (on the top and bottom halves of the circuit) is a legitimate choice. As can be seen from Fig. 2-26, an $\alpha$-transformation degrades the combiner's efficiency (positive incremental loss) over a significant portion of its operating range, assuming achievable component Quality factors remain unchanged by the transformation. On the other hand, the improvements in efficiency introduced by the $\beta$-transformation (involving the load) may be favorable depending on the application and actual operating range.

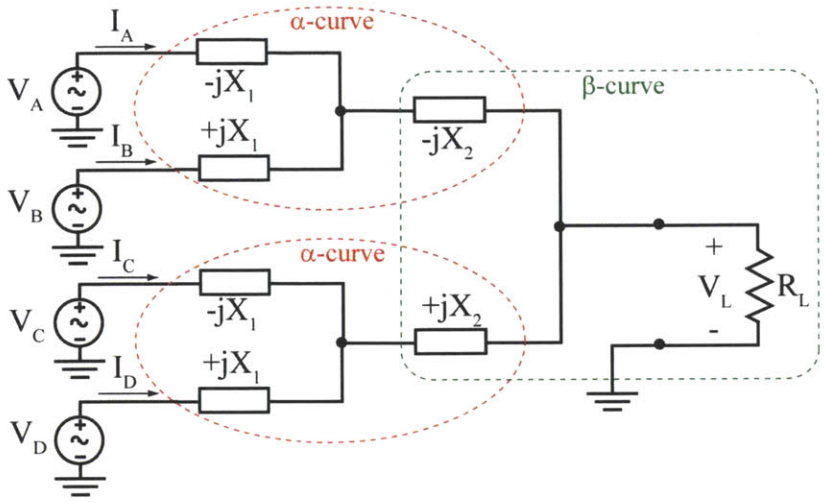



Fig. 2-25: Basic T-network implementation of a four-way power combiner along with outlined possible topological transformations and their corresponding incremental fractional loss curves in Fig. 2-26.

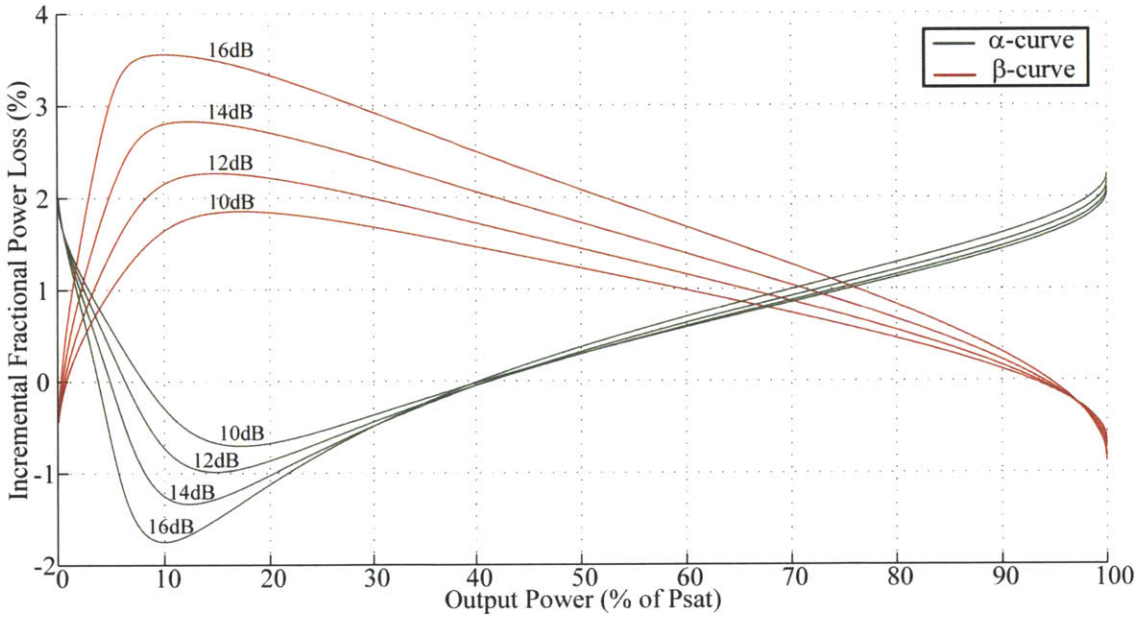



Fig. 2-26: Incremental fractional power loss curves for a four-way power combiner for various operating power range ratios versus output power (percentage of saturation power level).

## Chapter 3

# Implementation of a Power Combining and Outphasing System

The previous chapter has provided a detailed discussion on the theoretical fundamentals necessary for designing, analyzing, and understanding the operation of the proposed power combining architecture. In practice however, the experimental evaluation of the combiner's actual performance requires numerous additional components and systems such as power amplifiers, outphasing control systems, etc. The purpose of this chapter is to present a detailed design and implementation of an entire outphasing and power combining systems employing the already proposed combining architecture. The overall system architecture is first briefly overviewed along with its key performance specifications and additional components/sub-systems. The design and implementation of each individual sub-system is later explored in detail.

### 3.1. Overall System Architecture

In order to evaluate the performance of the proposed power combiner architecture and its feasibility in an actual combining system, the power combining and outphasing system of Fig. 3-1 is implemented. The system is designed to operate at a 27.12 MHz carrier (base) frequency - a common choice for many radio-frequency (RF) systems operating in the Industrial, Scientific, and Medical (ISM) band.

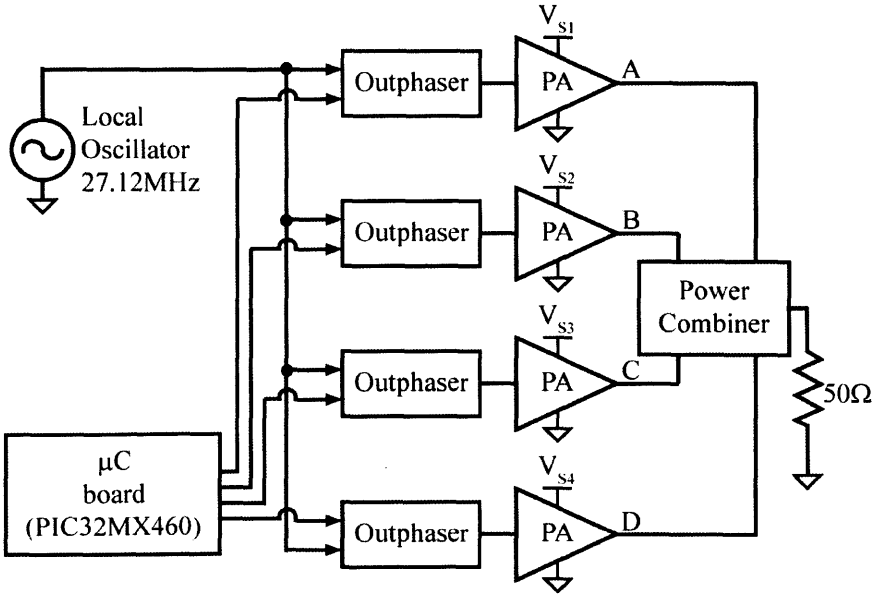



Fig. 3-1: Block diagram of the implemented power combining and outphasing system.

For the present system implementation, the four-way combiner of Fig. 2-5 is employed with branch reactances appropriately selected to provide an operation over approximately a 10 dB output power range (a 10:1 range of modulation in output power) and a 50 Ω loading impedance (a typical termination impedance for many RF systems). The input power ports of the combiner are driven by four identical class-E PAs which have been designed to deliver 25 W maximum output power at a 12.5 Ω load (when powered from a 16 V DC supply), and operate over a 10:1 load modulation ratio (12.5 Ω to 125 Ω) and corresponding power ratio [58]. Operation of the PAs over their full load-modulation and output power range (2.5 W to 25 W) allows one to achieve combiner output power levels in the range of 10 W to 100 W. (Since the combiner is not 100% efficient in reality, the output power of the PAs may have to be driven slightly above 25 W to achieve a total combiner output power of 100 W.)

In order to control the output power sourced from the PAs and delivered to the load, the PAs are outphased according to one of the outphasing control methods discussed above (IRCN, OS, and OP). This task is accomplished by employing specially designed outphasers which take a reference sinusoidal input from a 27.12 MHz local oscillator and output a phase-shifted version of the input, which in turn serves as the PA driving signal. All four outphasers use the same reference local oscillator (LO) signal, and the phase shift between the PAs is referenced to the LO signal. The amount of phase shift introduced by each outphaser is independently controlled (digitally) by a microcontroller (PIC32MX460, Microchip Technology Inc.) pre-programmed with a set of outphasing control angles (stored in a look-up table) corresponding to the desired output power levels. Moreover, if necessary, one is also able to manually adjust the phase of each PA in real-time. The design of the control system, the PAs, and the combiner are treated below.

## 3.2. Power Combiner Design and Implementation

### 3.2.1. Performance Specifications

For the purpose of demonstrating experimentally the proposed combiner architecture, the implementation of the four-way combiner of Fig. 2-5 has been selected. Approximately, a 10 dB operating power range (10 W to 100 W) has been chosen as a specification of the combiner prototype – a range that can not be easily achieved by conventional combining/amplification systems without suffering major power efficiency degradations. In addition, to comply with the traditional RF termination impedance practice, it is desired to design the combiner for a 50 Ω load. Fig. 3-2 illustrates the proposed combiner prototype specifications. The 10 dB operating power range refers to the power range between the outer two zero-points in the combiner's input admittance characteristic. Although the actual admittance characteristic depends on the particular outphasing control method employed (IRCN, OP or OS), the position of the zero-points remains unchanged with control methodology. Thus, for the specifications outlined here, one would desire the outer two combiner zero-points to be located at 10 W and 100 W respectively. One can see from

Fig. 2-12 that a 10 dB operating range corresponds approximately to 2° and 5° input admittance peak phase for OS/OP and IRCN outphasing control respectively. Although both control methods yield essentially a resistive PA loading, such peak phase estimates assumes that the combiner's reactive branches are perfectly tuned to the appropriate values, with the PAs outphased exactly according to Fig. 2-4. Determining the degree to which this can be achieved in practice is one of the objectives of the experimental evaluation of the proposed combiner prototype.

Moreover, since each of the PAs driving the combiner is designed to provide a 25 W peak output power at a 12.5 Ω load (with $25V_{pk}$ PA drive amplitude), the combiner must be designed in such way as to ensure that the effective PA loading at its highest zero-point (100 W) is 12.5 Ω. This implies that for a factor of ten in output power back-off, the combiner will present a ten times higher input resistance load to the PAs (125 Ω), which is consistent with their loading requirement at one-tenth of their peak output power level assuming the power amplifiers act as ideal voltage sources (i.e, voltage amplitude does not change with loading impedance).

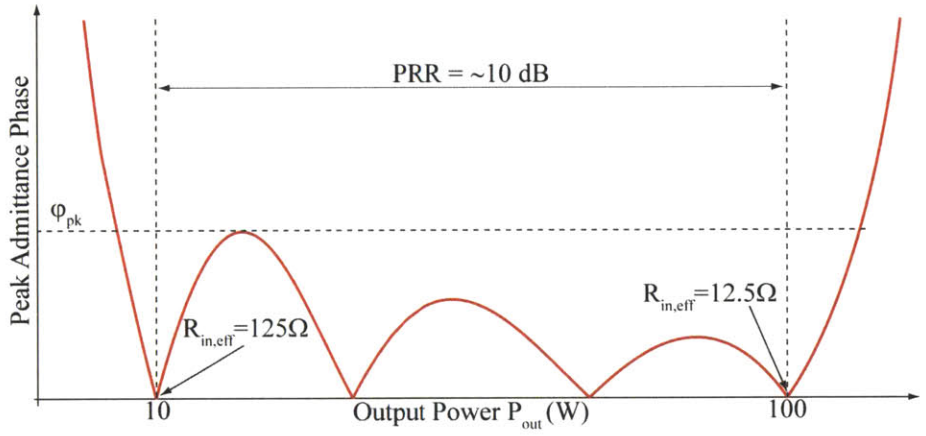



Fig. 3-2: Prototype combiner specifications: operation over a 10 W to 100 W (10 dB) power range with 125 Ω and 12.5 Ω effective loading resistance of the PAs at the outer two zero-points respectively. This curve is shown for IRCN control.

### 3.2.2. Combiner Design

It can be seen from the design curves illustrated in Fig. 2-12 that a 10 dB combiner operating range (between the outer two zero-points) corresponds to a design factor value of k = 1.053. Assuming a 50 Ω combiner loading impedance $R_L$, one can calculate the required combiner branch reactances $X_1$ and $X_2$ from (42) and (43) to be 35.2 Ω and 48.7 Ω respectively. The effective loading resistance $R_{100W}$ of each PA corresponding to the 100 W zero-point can now be calculated from (12.1) by replacing $R_{in,2,med}$ with $R_L$:

$$R_{100W} = \left( R_L + \sqrt{R_L^2 - X_2^2} - \sqrt{2R_L^2 - X_1^2 - X_2^2 + \frac{2R_L^3 - 2R_L X_2^2}{\sqrt{R_L^2 - X_2^2}}} \right) = 11.1\,\Omega \qquad (50)$$

However, as seen from (50), the effective PA loading at the 100 W zero-point is different from the desired 12.5 Ω loading. Consequently, one could scale the combiner reactances by factor of 12.5 Ω/11.1 Ω = 1.12 to ensure that $R_{100W}$ is indeed equal to 12.5 Ω. However, this would also require the combiner to see an effective loading impedance of 50 Ω*1.12 = 56.1 Ω at its output port. Since it is desired to use the combiner to drive a 50 Ω load, one could employ an impedance matching network (such as a transformer with the appropriate winding ratio) at the combiner's output port to transform the 50 Ω load to the desired 56.1 Ω. Although such a transformation ratio can be easily achieved in practice, it would only further complicate the system and introduce additional power loss.

Instead, a slightly different k-value of 1.042 can be chosen (at the cost of a slightly reduced power range) allowing the combiner to be loaded directly with 50 Ω, while satisfying the PA loading requirement of $R_{100W}$ = 12.5 Ω at the 100 W zero-point. The corresponding combiner output power range can be estimated to be 9.4 dB (from Fig. 2-12), with the outer two zero-points located at 100 W and 11.6 W. The branch reactances $X_1$ and $X_2$ for k = 1.042 can be calculate from (43) and (43) to be 36.69 Ω and 48.97 Ω respectively. Fig. 3-3 shows the expected effective combiner input admittance over its operating range for k = 1.042 and $R_L$ = 50 Ω under OP outphasing control. As can be seen from the conductance plot, the combiner presents a resistive PA loading of 125 Ω and 12.5 Ω respectively at 10 W and 100 W, satisfying the PA loading requirement.

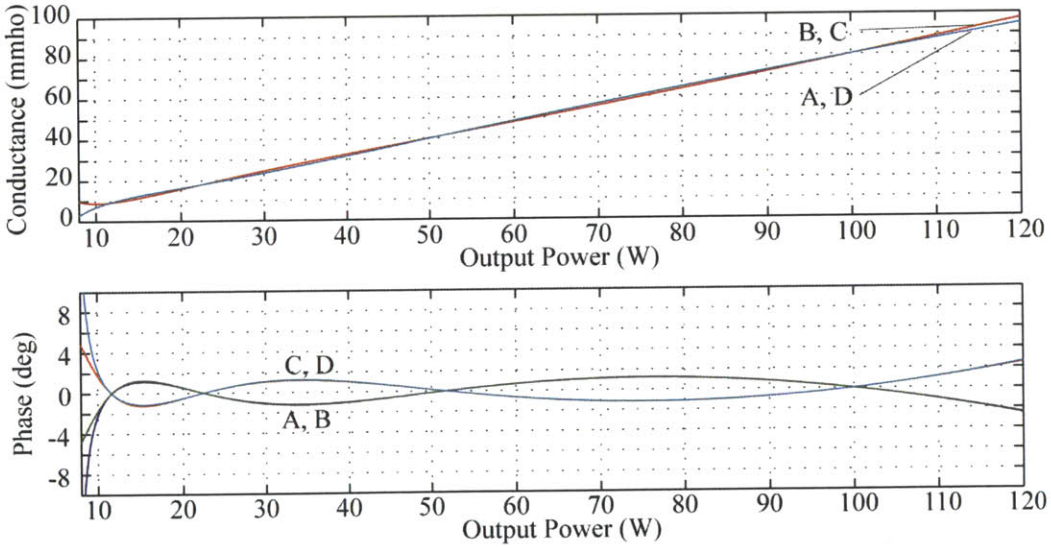



Fig. 3-3: Effective input conductance (top), and phase (bottom) seen by each of the PAs (A-D) driving the four-way combiner of Fig. 2-5 with $R_L$ = 50 Ω, $X_1$ = 36.69 Ω, and $X_2$ = 48.97 Ω (k = 1.042) as a result of OP outphasing control.

### 3.2.3. Combiner Implementation

Each of the combiner reactances $X_1$ and $X_2$ (see Fig. 2-5) were realized with a series combination of an inductor and a capacitor. This implementation blocks any direct-current (DC) paths from the combiner's

input ports to its output port, and helps suppress any harmonic content from the PAs. Moreover, it facilitates combiner tuning: any branch reactance can be easily adjusted by simply adding some extra capacitance in parallel with the already mounted branch capacitor. Fig. 3-4 depicts the actual combiner implementation.

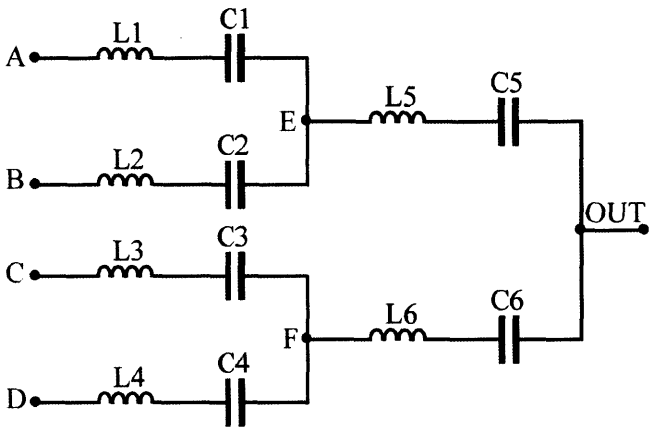



Fig. 3-4: Power combiner implementation. Each of the reactive branches in Fig. 2-5 is realized with an L/C series combination.

It was shown in the previous subsection that the desired branch reactance values for $X_1$ and $X_2$ are respectively 36.69 Ω and 48.97 Ω. The values of the inductors and capacitors in Fig. 3-4 have been selected appropriately to yield the required branch reactances at the combiner's operating frequency of 27.12 MHz. It is important to properly tune the combiner (adjust the $X_1$ and $X_2$ reactances to their intended values), as the combiner's performance is very sensitive to variations in the reactance values. Even a 5% deviation in the reactance values may result in noticeable degradations to the combiner's input admittance characteristic and considerable variation in the input admittance phase/susceptance. A simple methodology employed in tuning the combiner is briefly described in the subsequent section. All of the employed components are readily available off-the-shelf and are summarized in Table I. Fig. 3-5 shows a photograph of the tuned combiner PCB, while Appendix D.2 provides the PCB artwork.

TABLE I: POWER COMBINER COMPONENT VALUES

| Component | Value | Part # | Manufacturer |
|---|---|---|---|
| L1, L3 | 222 nH | 132-14SMJL | Coilcraft Inc. |
| L2, L4 | 422 nH | 132-18SMJL | |
| L5 | 307 nH | 132-16SMJL | |
| L6 | 538 nH | 132-20SMJL | |
| X1-X7 | 3.3 uH | 7M2-332 | |
| C1, C3 | 78.8 pF | ATC100B Capacitor Series | American Technical Ceramics Corp. |
| C2, C4 | 167 pF | | |
| C5 | 57.9 pF | | |
| C6 | 137 pF | | |

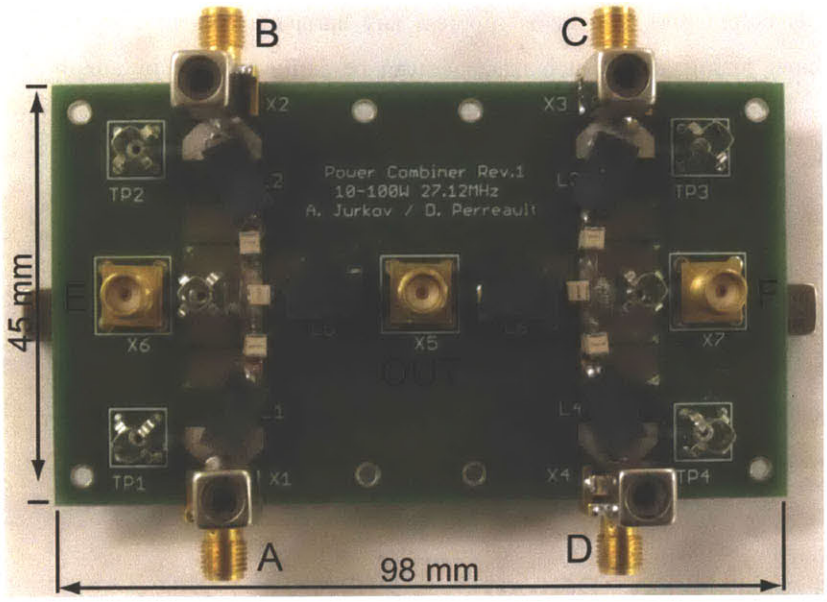



Fig. 3-5: Photograph of the tuned four-way combiner PCB with its four input ports A-D and single output port OUT. Ports E and F are used only for tuning the combiner.

It is of interest to monitor the voltage waveforms at the combiner's input ports, and so, oscilloscope probe connectors (Part #: 131-4244-00, Tektronix Inc.) have been mounted in parallel with the SMA input-port connectors (TP1-TP4 in Fig. 3-5). However, the resultant parasitic capacitance (approximately 15 pF) at each of the combiner's input ports (the parallel combination of the SMA connector and the oscilloscope probe capacitances) can considerably affect the performance of the combiner and alter its input-impedance characteristics. To address this issue, tunable inductors (7M2-332, Coilcraft Inc.) with a nominal inductance of 3.3 μH are installed in parallel with the probe connectors (X1-X4, Fig. 3-5) to "resonate out" the parasitic capacitances at 27.12 MHz. Although there is some small parasitic capacitance associated with the other nodes of the power combiner circuit, their value has been measured to be no greater than 3 pF, and so their affect on the combiner's characteristics is negligible. Note however that during the combiner tuning procedure (to be described shortly), oscilloscope probes are temporarily connected to ports E and F to monitor the voltage waveforms. In order to "resonate-out" the probes' parasitic capacitances, similar tuning inductors are temporarily installed in parallel with the probes, and are removed once after the tuning procedure is completed.

Since the proposed power combiner is implemented entirely with reactive components, it is ideally lossless. However, due to the finite Q-factor of the used components, and hence small, but non-zero parasitic resistance of the capacitors and inductors, some resistive combiner power loss is expected depending on the combiner's operating point and the respective combiner branch currents. It is useful to briefly examine the effect of the components' finite Q-factor on the combiner's efficiency.

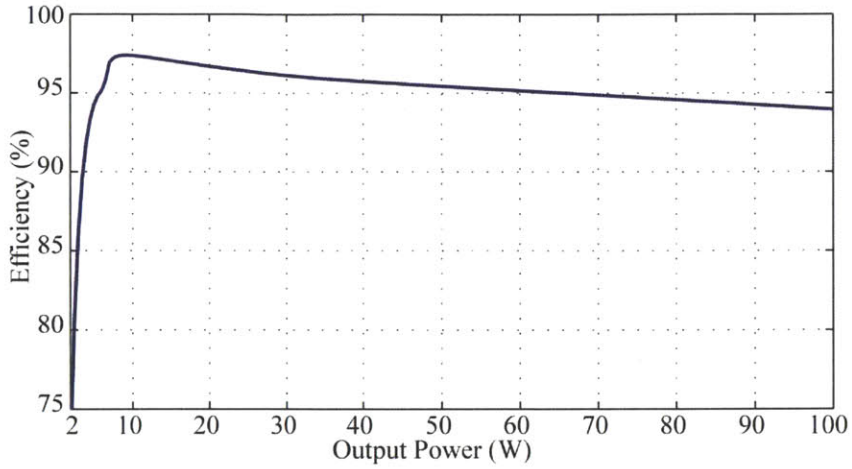



Fig. 3-6: Simulated combiner efficiency including Q-factor losses.

According to the respective manufacturer's component datasheets, at the current system operating frequency (27.12 MHz) inductors L1-L6 (see Fig. 3-4) have an approximate Q-factor of 90, while the tunable inductors X1-X4 have a Q-factor of 25. Capacitors C1-C6 have a much higher Q-factor (greater than 10,000), and so their resistive losses are negligible as compared to those of the inductors. Fig. 3-6 depicts the simulated efficiency of the combiner due solely to resistive power losses associated with the component's finite Q-factors

### 3.2.4. Combiner Tuning

The behavior of the combiner is strongly dependent on its branch reactances, and variations or mismatches in their values could dramatically alter the combiner's resistive input admittance characteristics by introducing significant PA reactive loading. This in turn could have significant detrimental effects to the performance and efficiency of the overall power amplification and combining system. Thus, before using the combiner, it is important to tune its branch reactances to their appropriate values (determined by design) at the combiner's operating frequency (27.12 MHz). This subsection describes the tuning procedure undertaken and outlines the steps followed to assemble the combiner board.

The first step is to "resonate-out" the parasitic capacitance associated with the SMA port connectors and the oscilloscope probes that are to be used in monitoring the port voltage waveforms. Starting with an unpopulated combiner PCB (see Appendix D.2 for PCB artwork), firstly, only the SMA connectors (A-F), the oscilloscope probe connectors (TP1-TP7), and the tunable can inductors (X1-X7) are populated (see Fig. 3-5). Beginning with port A, a 10 MΩ, 8 pF oscilloscope probe (P6139A, Tektronix Inc.) is connected to TP1. The port A input impedance is measured with an impedance analyzer (4935A, Agilent Technologies Inc.). The tuning inductor X1 is then adjusted until the port A input impedance peaks at 27.12 MHz. For the present combiner, a peak input port impedance of approximately 2.5 kΩ has been achieved with the tuning inductor having a Q-factor of 25. This procedure is repeated for each of the remaining ports B-F.

Populating the rest of the combine PCB proceeds by first mounting C5, C6, L5, and L6. Initially, slightly lower values for C5 and C6 are used (for example, 5% less than what is required). Ports E and F are loaded with 50Ω (462-1, MECA Electronics Inc.). A 27.12 MHz, 2 Vpp sinusoidal signal is injected into the output port (OUT) of the combiner using a waveform generator (33250A, Agilent Technologies Inc.). The voltage waveforms at ports E and F are monitored by connecting two 10 MΩ, 8 pF oscilloscope probes (P6139A, Tektronix Inc.) to TP6 and TP7 respectively. Small capacitance increments are added in parallel with C5 and C6 (for example, 1 pF increments) until the waveforms at ports E and F have the same amplitude, and a relative phase shift determined by the desired branch reactance value. The actual amplitude of the injected sinusoidal signal is not of significant importance as long as the output voltage waveforms at ports E and F are within the input range of the oscilloscope and can be measured with an appreciable resolution. Here, one should be concerned only with the relative phase and amplitude of the voltage waveforms at ports E and F. To understand better the nature of the employed tuning methodology, consider Fig. 3-7 illustrating the tuning set-up described above. The voltages $v_e$ and $v_f$ at ports E and F (expressed as phasors) are given by (51) as a function of the injected signal $v_{in}$.

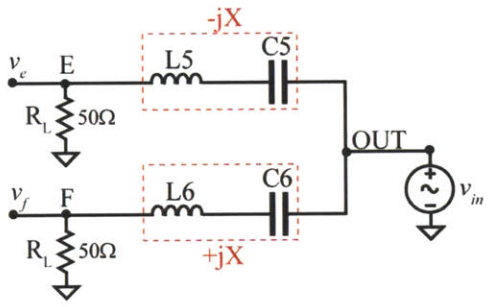



Fig. 3-7: Tuning set-up for tuning the L5/C5 and L6/C6 combiner reactive branches. Ports E and F are loaded with $R_L$ = 50 Ω, while a 27.12 MHz test signal is injected at the combiner's OUT terminal.

$$\begin{aligned} V_e &= V_{in}\frac{R_L}{\sqrt{R_L^2+X^2}}\exp\left(j\tan^{-1}\left(\frac{X}{R_L}\right)\right) \\ V_f &= V_{in}\frac{R_L}{\sqrt{R_L^2+X^2}}\exp\left(-j\tan^{-1}\left(\frac{X}{R_L}\right)\right) \end{aligned} \tag{51}$$

As can be seen from (51), $v_e$ and $v_f$ have equal amplitudes only when the L5/C5 and L6/C6 branch reactance magnitudes match (are equal). Furthermore, to achieve the desired branch reactance value, the C5 and C6 values must be adjusted until the right relative phase between $v_e$ and $v_f$ is obtained. In the case of the L5/C5 and L6/C6 branches, it is desired to obtain X = 48.97 Ω. Thus, from (51) the relative phase between $v_e$ and $v_f$ must be $2*\tan^{-1}(X/R_L) = 88.8°$.

Once the L5/C5 and L6/C6 branches are tuned, the PCB copper traces connecting C5 and C6 to TP5 and TP6 (see Fig. 3-5) respectively are removed to prevent any undesirable loading to the summing nodes E and F. An analogous tuning procedure is applied to branches L1/C1 and L2/C2, and branches L3/C3 and L4/C4 with a sinusoidal signal injected respectively into ports E and F.

## 3.3. Power Amplifiers

In applications involving frequencies above 10 MHz, single-switch power amplifiers (or resonant inverters) such as the Class-E inverter are often preferred. Fig. 3-8 depicts the topology of the 27.12 MHz Class-E amplifiers employed for driving the combiner. The input inductor $L_F$ acts as a choke, while the parallel-tuned output filter network $L_P$-$C_P$ improves the output waveform quality by attenuating higher-frequency components. (Note that the combiner is designed to operate at a very narrow bandwidth, with the input-port voltage waveforms ideally being sinusoidal.) In a traditional Class-E inverter [33, 34, 59] the tuned load network comprising $C_S$, $L_S$, the total drain-to-source capacitance $C_F$ (the combination of $C_D$ and the switch output capacitance $C_{OSS}$), and the inverter's loading impedance $R_o$ (in this case, the effective combiner input-port impedance) are selected to shape the drain-to-source switch voltage $v_{DS}$ to provide zero-voltage switching (ZVS) and zero $dv_{DS}/dt$ switch turn-on.

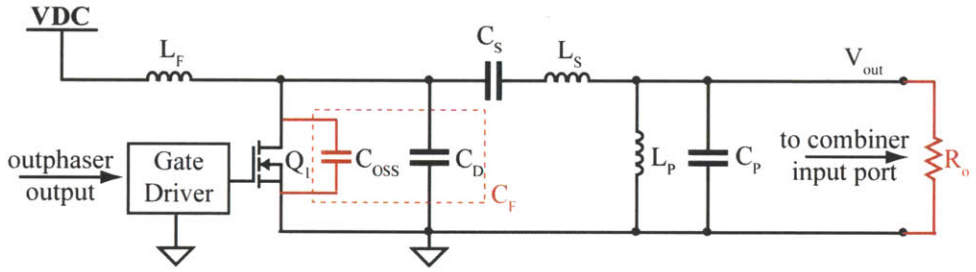



Fig. 3-8: Topology of the implemented Class-E power amplifier.

Since the transistor's drain voltage waveform is shaped by the load network, the traditional Class-E inverter is highly sensitive to loading variations [34, 52], and considerably deviates from zero-voltage switching for load resistance variations of more than about a factor of two. Since in the present application, the input-port combiner impedance is modulated over a 10:1 range, a recently proposed Class-E design methodology was employed for selecting the inverter components ($L_S$, $C_S$, $L_P$, $C_P$, and $C_F$) so as to maintain zero-voltage switching and constant switch duty-ratio over the entire load-modulation range, without necessarily ensuring a zero $dv_{DS}/dt$ switch turn-on as loading resistance varies [58]. This design methodology is outlined below.

The design of the PA (inverter) for load modulation begins by a set of performance specifications: resonant (switching) frequency $f_1$, rated output power $P_{or}$ (at rated load $R_{or}$), and load resistance modulation range (from minimum load resistance $R_{min}$ to maximum load resistance $R_{max}$). The purpose of the employed design methodology is to select the input network components ($L_F$ and $C_F$), and the output network components ($L_S$, $C_S$, $L_P$, and $C_P$) based on the given specifications. For the present power combining and outphasing system design, the required PA specifications are listed in Table II.

TABLE II: PA DESIGN SPECIFICATIONS

| Parameter | Value |
|---|---|
| Rated load resistance $R_{or} = R_{min}$ | 12.5 Ω |
| Rated output power $P_{or}$ | 25 W |
| Switching frequency $f_1$ | 27.12 MHz |

It can be shown that load resistance $R_o$, dc supply voltage $V_{DC}$, and output power $P_o$ are related approximately by (52):

$$P_o = 1.32\frac{V_{DC}^2}{R} \tag{52}$$

Furthermore, the PA output voltage amplitude $V_o$ is approximately invariant to modulation of its loading resistance and is determined by the supply voltage ($V_{o,rms} \approx 1.15V_{DC}$). Thus the minimum and maximum output power levels are set by $R_{max}$ and $R_{min}$ respectively. From (52) and the specifications given in Table II, one can calculate that the required DC supply voltage is approximately 16 V.

It has been observed that in order for the PA to exhibit good power efficiency under load modulation, it is desirable for the load network impedance to remain resistive as loading varies. Thus, one must tune the $L_S/C_S$ and $L_P/C_P$ networks to for resonance at the switching frequency (53):

$$\frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_S C_S}} = 2\pi f_1 \tag{53}$$

The characteristic impedances of the $L_S/C_S$ and $L_P/C_P$ networks is selected such as to provide sufficient filtering of the output voltage. While highly application dependent, for the present design a $Q_{fil}$ of approximately 5 is selected.

$$\frac{\sqrt{L_S / C_S}}{R_{min}} = \frac{R_{max}}{\sqrt{L_P / C_P}} = Q_{fil} \tag{54}$$

On the other hand, tuning the input-side $L_F/C_F$ network just slightly below 1.5 times the switching frequency (55) allows one to achieve the desired soft-switching performance.

$$\frac{1}{\sqrt{L_F C_F}} = 3\pi f_1 \tag{55}$$

The characteristic impedance of the $L_F/C_F$ network is in turn selected based on the rated (minimum) load resistance (56) where $k_f$ is a design constant and its value is typically selected between 0.5 and 1.5.

$$\sqrt{L_F / C_F} = k_f R_{min} \tag{56}$$

Detailed design of the PA for the specifications in Table II, by employing the method outlined above, is presented in [58]. The PA design that served as the basis for this system was largely undertaken by Mr. Lukasz Roslaniec, a visiting graduate student at MIT. Table III summarizes the PA components along with their implementation.

TABLE III: COMPONENT VALUES AND THEIR IMPLEMENTATION FOR THE CLASS-E PA

| Component | Value | Implementation |
|---|---|---|
| $L_F$ | 35.6 nH | 3 parallel 132-09SMJL inductors (Coilcraft Inc.) |
| $L_S$ | 380 nH | 132-17SMJL inductor (Coilcraft Inc.) |
| $L_P$ | 169 nH | 132-12SMJL inductor (Coilcraft Inc.) |
| $C_D$ | 377 pF | ATC700A Capacitor Series (American Technical Ceramics Corp.) |
| $C_S$ | 90 pF | |
| $C_P$ | 203 pF | |
| $Q_1$ | $C_{oss} \approx 150$ pF<br>$R_{on} \approx 0.03\ \Omega$ | EPC1007 (Efficient Power Conversion Corp.) |

The gate-driving circuit is shown in Fig. 3-9. Its purpose is to take the properly phase-shifted drive signal generated by the outphasers and condition them for driving the gate of the PA transistor. Due to the non-linear mixing process employed by the outphaser, significant harmonic content is introduced in the phase-shifted signal (see Fig. 3-10). The outphaser output signal is band-pass filtered at 27.12 MHz to isolate only the fundamental and correctly phase-shifted component. The sinusoidal filter output is then "squared" with a comparator (LT1719, Linear Technology Inc.) and fed to a 3:1 tapered inverter driver (NC7WZ04, Fairchild Semiconductor Inc.), which in turn drives directly the gate of the MOS transistor. Fig. 3-10 shows the gate-drive signal $V_{gs}$ generated by the gate driver having nearly 50% duty-cycle and relatively fast rise and fall times (~ 2 ns). Note that the implemented gate-driving circuit conveniently ensures the same gate signal duty-cycle irrelevant of the amplitude and phase of the outphaser's output signal.

Lastly, it should be noted that in many RF applications incorporating switched-mode power amplifiers, it is desirable to be able to use drive amplitude modulation to enable power to be reduced continuously down to zero (albeit with poor efficiency). This particular prototype does not allow for such operation owing to the structure of the selected gate drive. However, such capability could be easily introduced.

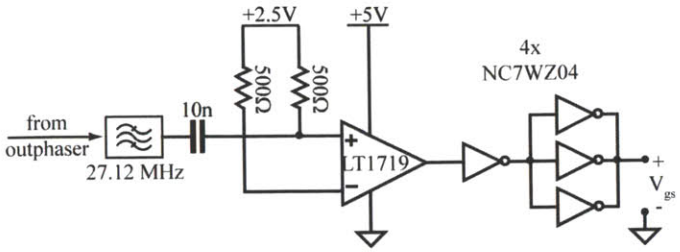



Fig. 3-9: Circuit schematic of the gate-driver employed in the PA of Fig. 3-8.

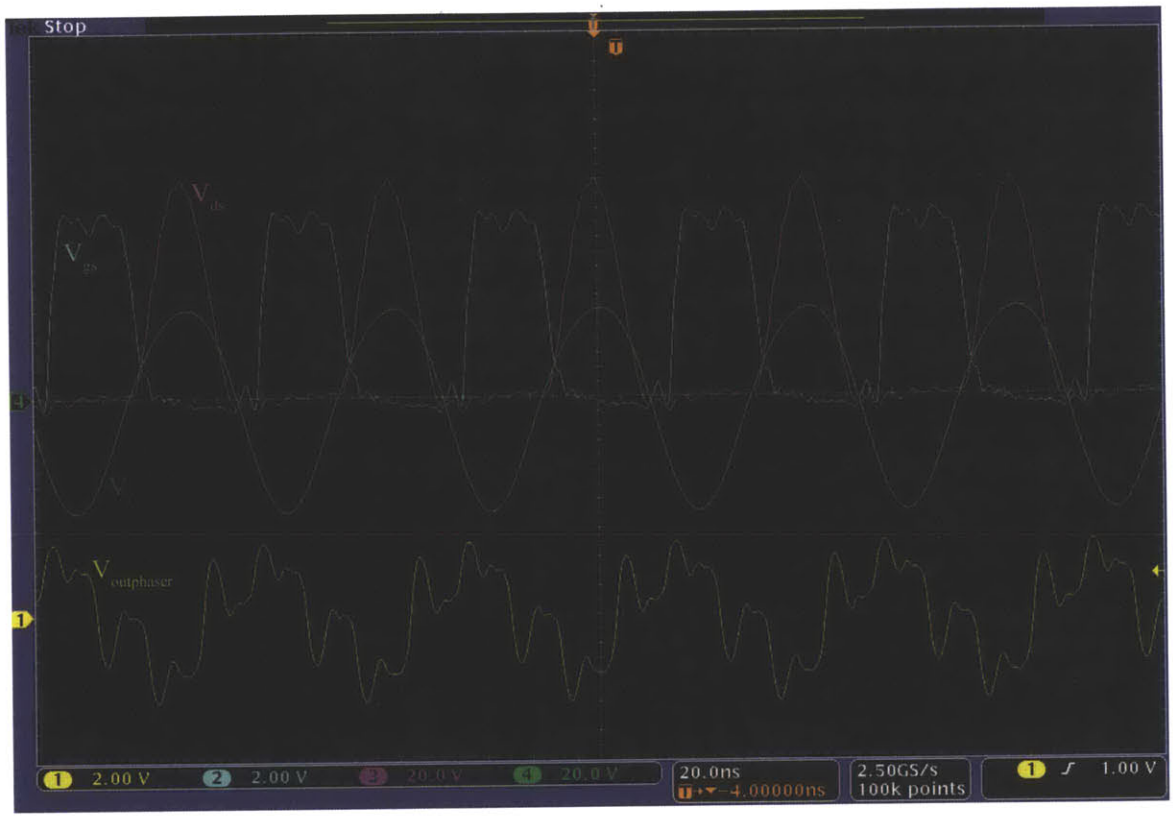



Fig. 3-10: Oscilloscope screenshot showing key voltage waveforms of a PA driving a 50 Ω load and powered by a supply voltage of 16 $V_{DC}$. Channel 1: outphaser output $V_{outphaser}$ (input to the gate-drive circuit), Channel 2: gate-drive signal $V_{gs}$, Channel 3: drain voltage $V_{ds}$, and Channel 4: PA output waveform $V_o$.

Furthermore, one can clearly see from Fig. 3-10 that the transistor is indeed soft-switching at turn-on: the drain voltage $V_{ds}$ returns to zero just before the transistor is turned on. Moreover, the PA output waveform is nearly sinusoidal with amplitude of approximately 26 V corresponding to an output power of 6 W with the PA driving a 50 Ω load.

For illustrative purposes, Fig. 3-11 shows a photograph of the implementation of a single Class-E PA, clearly outlining the gate driver circuit. The outphaser's output is fed to the PA's IN port, while its OUT port connects directly to one of the four power combiner input ports. The PCB artwork and the detailed schematic are included in Appendix D.3.

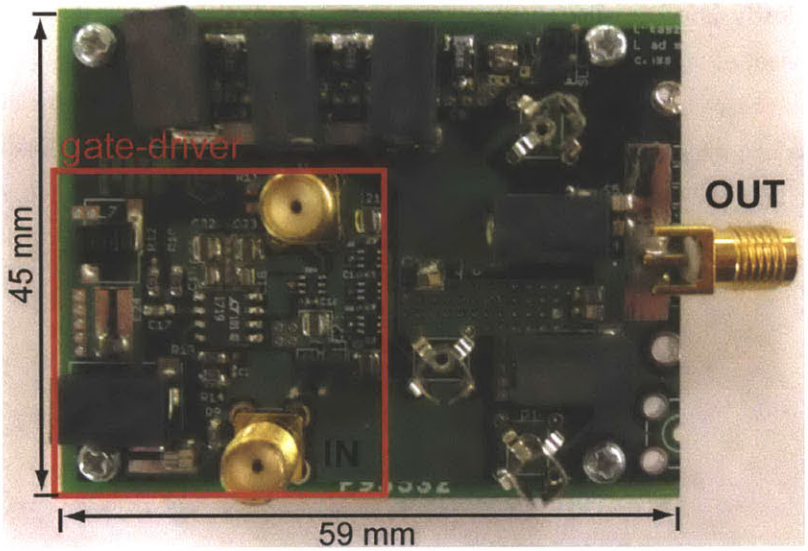



Fig. 3-11: Photograph of a single implemented Class-E PA PCB.

## 3.4. Outphasers

As described previously, the purpose of the outphasers is to introduce the desired phase-shift in each of the PA drive signals and thus control the combiner's output power. The outphasers are designed to operate over a very wide bandwidth (5 MHz - 200 MHz) in order to facilitate the eventual testing of power combiners operating at various frequencies while alleviating the necessity for significant system modifications and redesign. The outphaser implementation discussed here is capable of providing any desired phase shift from -180° to 180° with an accuracy of approximately ±0.1° over the entire bandwidth. This is achieved by employing an In-phase/Quadrature (IQ) Modulator (LTC5598, Linear Technology). An IQ modulator allows one to effectively outphase a reference local oscillator (LO) signal by an amount determined by the in-phase (I) and the quadrature (Q) components. The fundamental operation of an I/Q modulator is illustrated in Fig. 3-12. The LO input signal is phase shifted to create two orthogonal signals cos(ωt) and sin(ωt) having the same frequency as the LO signal. They are in turn mixed respectively with the I and Q input signals, and the resulting signals are summed to produce the I/Q modulator output.

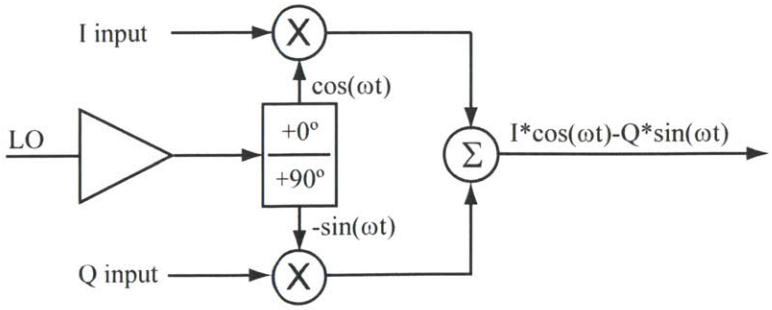



Fig. 3-12: Block diagram of a hypothetical IQ modulator.

Fig. 3-13 clearly illustrates the phasor relationship between the LO signal, and the fundamental frequency component of the I/Q modulator output (the RF signal). By appropriately adjusting I and Q the RF signal can be phase-shifted by any arbitrary amount with respect to the LO signal. The employed LTC5598 I/Q modulator has differential I and Q inputs, and in order to minimize modulation distortions, it requires that both the I and Q signals be limited to a 1 $V_{pp}$ differential range (-0.5 V to +0.5V).

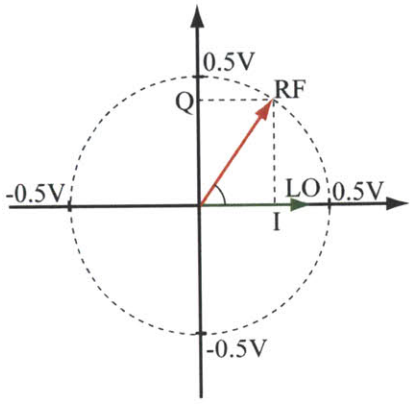



Fig. 3-13: Phasor representation of the I/Q modulator output signal (RF) and its reference local oscillator input (LO).

An overall block diagram of the outphaser is shown in Fig. 3-14. A 2-channel, 12-bit DAC (DAC5662, Texas Instruments Inc.) is used to generate the I and Q components. Although the maximum sampling rate of the DAC is limited to 275 MSPS, 1 MHz low-pass filters are installed on each of its two analog output channels to filter-out the DAC sampling frequency components and limit the I and Q signal bandwidths to less than 1 MHz. This bandwidth is more than sufficient for the purpose of evaluating the quasi-static behavior of the power combining system presented here. Nevertheless, if higher I and Q signal bandwidths are desired, one can simply replace the filter's inductors (L2 and L3) and capacitors (C4-C7) to achieve a higher cut-off frequency (see Appendix D.1 for detailed outphaser schematic).

The DAC has been configured to operate in the interleaved data mode. In this mode of operation, a single 12-bit digital bus is used to program both of the DAC's 12-bit channels. External clock signals are required to synchronize the programming and update of the DAC's analog channels. A PIC32MX460 microcontroller-based development board (LV-32MX, MikroElektronika) is responsible for controlling all outphasers and program their corresponding DACs. Since however, the micro-controller board and the DACs have different supply and logic level voltages, three digital four-channel isolators (SI8440, Silicon Labs) are installed on the 12-bit DAC data bus.

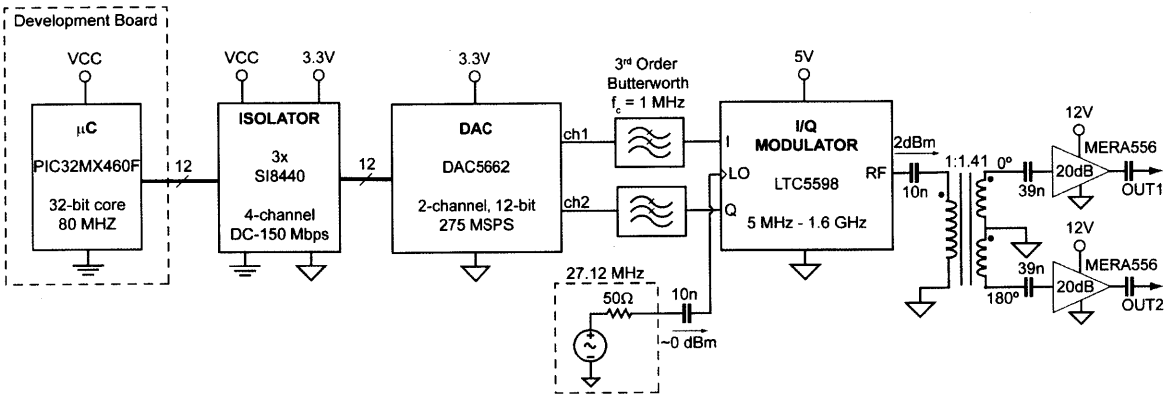



Fig. 3-14: Block diagram of the outphaser.

On the output side of the I/Q modulator, the RF signal is coupled to a balun (T2-1T, Mini-Circuits) with a 1:2 impedance ratio (1:1.414 primary-to-secondary turns ratio) thus producing two complementary (180° apart) versions of the RF signal, each further amplified by a 20 dB gain stage (MERA556, Mini-Circuits). Each gain stage has 50 Ω input impedance, effectively resulting in a 100 Ω load for the balun's secondary winding. Since the balun has a 1:2 impedance transformation ratio, the RF output port of the I/Q modulator is effectively loaded with 50 Ω in accordance with its termination requirements. The two complementary outphaser outputs OUT1 and OUT2 allow the outphaser to be used with PAs requiring complementary gate-driving signals (such as a Class-B push-pull stage). Note however that in the present work only one of the outputs is used (OUT1 in Fig. 3-14) while the other is terminated with 50Ω. Due to the non-linear mixing process incorporated inside the modulator to introduce the desired phase shift, its output contains significant harmonic content, and so, a 27.12 MHz band-pass filter (part of the PA gate-driving circuit, discussed in subsection 3.3) must be used to extract the fundamental component from OUT1, which in turn, is coupled directly to the PA gate drivers (see Fig. 3-9).

A set of jumpers (J3-J6, outphaser PCB schematic, Appendix D.1) is used to pre-select the operating mode of the outphaser and some of its components. The configuration of the jumpers for the present power combing and outphasing system, along with a brief description is included in Table IV. Refer to Appendix D.1 for a detailed outphaser schematic and PCB artwork along with the various jumpers and their pins. Fig. 3-15 shows a photograph of a single assembled outphaser board.

TABLE IV: OUTPHASER JUMPER CONFIGURATION

| Jumper | Configuration | Description |
|---|---|---|
| J3 | 2-3 | Set DAC for interleaved mode operation |
| J4 | 1-2 | Set DAC to internally equalize the gain of both analog output channels |
| J5 | 2-3 | Disable DAC sleep mode |
| J6 | 2-3 | Enable I/Q modulator |

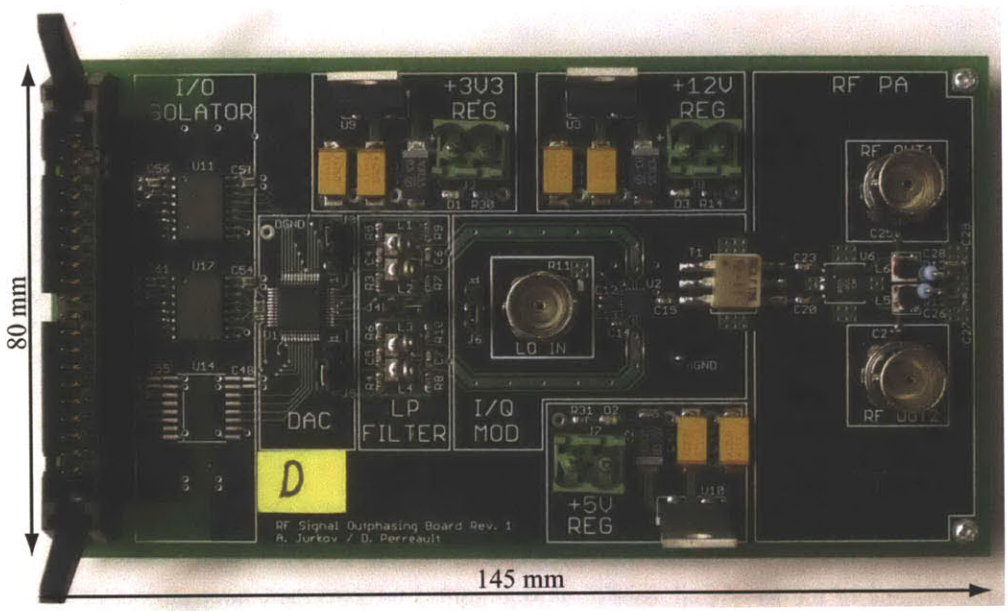



Fig. 3-15: Photograph of an assembled outphaser board. The entire power combining system employs four such boards, each responsible for phase-shifting its corresponding PA.

### 3.4.1. Outphaser Control and DAC Programming

The amount of phase introduced by the outphaser in the PA drive signal is controlled by appropriately programming the DAC to produce the required I and Q values used by the I/Q modulator. The phase $\varphi$ between the modulator's reference LO signal and the fundamental harmonic component of its output is given by (57):

$$\varphi = tan^{-1}\left(\frac{V_Q}{V_I}\right) \tag{57}$$

where $V_Q$ and $V_I$ are the differential voltages at the I and Q inputs of the modulator respectively. Note that the employed DAC is a current-mode DAC, i.e. programming the DAC sets the output current of each of its two analog outputs. External resistors (see the outphaser schematic, Appendix D.1) are used to convert these currents to the necessary differential voltages $V_Q$ and $V_I$ to drive the modulator. For the present outphaser design, $V_I$ and $V_Q$ are approximately given by (58), where CODE_I and CODE_Q are the 12-bit digital codes programmed into the DAC respectively for the I and Q channels [62]. The DAC reference voltage $V_{ref}$ is set to approximately 1 V.

$$\begin{aligned} V_I &= V_{ref}\left[\frac{2*CODE\_I - 4095}{4096}\right] \\ V_Q &= V_{ref}\left[\frac{2*CODE\_Q - 4095}{4096}\right] \end{aligned} \tag{58}$$

In the present outphaser design, the DAC is configured to be programmed over a single 12-bit bus D[11:0]. Thus, in order to program both of its channels and synchronize their output update rate, a few external control signals are required. Fig. 3-16 illustrates the implemented signal timing diagram for a single DAC programming cycle.

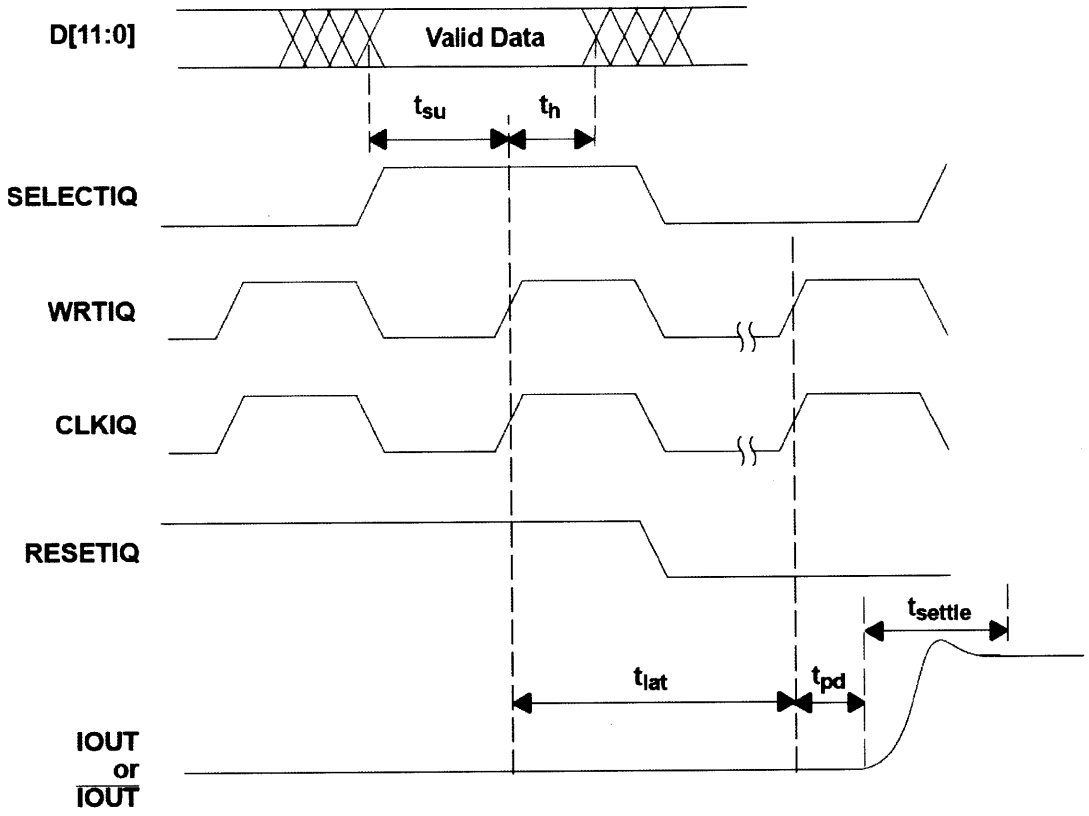



Fig. 3-16: Control signal timing diagram for programming the DAC in the single-bus interleaved operating mode [62].

The SELECTIQ signal allows the selection of the channel (1 - I, 0 - Q) that one desires to program. The channel code on the digital bus (CODE_I or CODE_Q) is latched into the selected channel register on a rising edge of CLKIQ and WRTIQ. Both DAC outputs are updated simultaneously on a rising edge of WRTIQ and CLKIQ when RESETIQ = 0. The set-up time $t_{su}$, hold time $t_h$, clock latency $t_{lat}$, propagation delay $t_{pd}$, and output settling time $t_{settle}$ are summarized in Table V [62].

TABLE V: DAC CONTROL SIGNAL TIMING PARAMETERS

| Parameter | Value |
|---|---|
| Set-up time $t_{su}$ | 0.5 ns |
| Hold time $t_h$ | 0.5 ns |
| Clock latency $t_{lat}$ | 4 CLKIQ cycles |
| Propagation delay $t_{pd}$ | 1.5 ns |
| Settling time $t_{settle}$ | 20 ns |

### 3.4.2. DAC Calibration

Although (58) gives the ideal relationship between the channel programming CODE word and the respective channel output voltage, the DAC reference voltage is set by an external resistor, and so, its value may differ from one outphaser to another. For better accuracy in the DAC's transfer function, it is desirable to calibrate (empirically determine) the conversion relation once the outphaser boards are fully assembled. The calibration process entails programming each of the DAC's channels with a set of 12-bit reference CODE words spread over the entire DAC conversion range. The differential voltage at the DAC's output channels is measured for each of the programmed codes, and a best-fit straight line is constructed through the measured points (59):

$$CODE\_IQ = M_{IQ} V_{IQ} + B_{IQ} \tag{59}$$

where $V_{IQ}$ is the differential voltage (in mV) at the I or Q channels, and CODE_IQ is the corresponding channel programming word. The values of constants $M_{IQ}$ and $B_{IQ}$ are measured empirically for both the I and Q channels. This calibration procedure is repeated for each of the four outphaser boards (A-D). For the four implemented outphasers, these calibration constants are empirically determined and summarized in Table VI.

TABLE VI: DAC CALIBRATION CONSTANTS FOR EACH OF THE OUTPHASER BOARDS

| Calibration Constant | Outphaser Board | | | |
|---|---|---|---|---|
| | A | B | C | D |
| $M_I$ | 2.1830 | 2.1959 | 2.2135 | 2.1780 |
| $M_Q$ | 2.2072 | 2.2115 | 2.2339 | 2.1867 |
| $B_I$ | 2047.4 | 2047.5 | 2047.4 | 2047.8 |
| $B_Q$ | 2047.7 | 2047.8 | 2047.3 | 2047.1 |

## 3.5. System Control

A PIC32MX460 microcontroller (Microchip Technology Inc.) is utilized to control the four outphaser boards, and thus adjust the relative phase shift between the PAs driving the combiner. In order to facilitate the rapid prototyping of various control schemes without the requirement for major hardware redesign, an off-the-shelf development board (Fig. 3-17) was used (LV32MX v6, MikroElektronika). The four outphaser boards are connected to the appropriate microcontroller pins through the factory-installed development board connectors. The mapping of the various outphaser board control signals to the development board pins is provided for each of the outphasers A-D in Table VII.

A simple firmware is developed for the microcontroller which allows one to adjust the outphasing of the PAs and in turn control the combiner's output power. The appropriate outphasing angles for each PA for various combiner output power levels are stored in a look-up table on the microcontroller's memory. Through a couple of push-buttons located on the development board, one can communicate with the microcontroller and cycle through the various outphasing angle settings. Moreover, the firmware allows for

manual, real-time independent adjustments to the phase shift of each PA within increments of less than 0.1°. This feature is particularly useful for administering fine phase shift adjustment to the already pre-programmed angles to calibrate-out any non-symmetric time delays introduced in the PA signal path. However, it may be also used to adjust the PA outphasing angles to any desired value, and thus achieve combiner output power levels other than the ones already pre-programmed in the microcontroller. A state-diagram of the developed firmware is shown in Fig. 3-18. A total of six push-buttons located on the development board (RC1-RC4, and RA14-RA15) are used to issue various commands to the microcontroller.

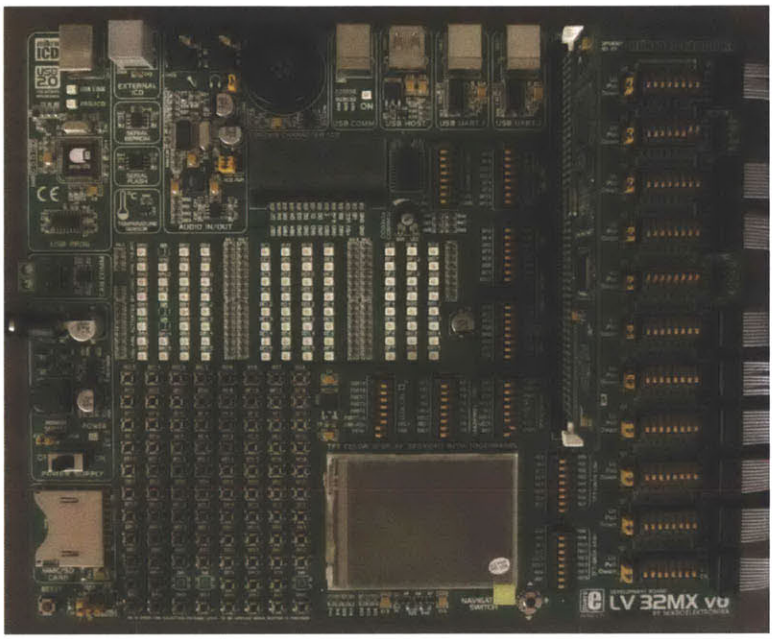



Fig. 3-17: Photo of the PIC32MX460-based development board (LV32MX, MikroElektronika).

Upon a system power-on, or restart, the microcontroller automatically initializes the PA outphasing angles to values corresponding to the lowest combiner output power level of 10 W. By using push-buttons RA14 and RA15, once can cycles through the pre-programmed list of PA outphasing angle pairs. On the other hand, push-buttons RC1 and RC2 can be used to select a particular PA for manual phase shift adjustment. Push-buttons RC4 and RC3 increment and decrement respectively the particular PA phase shift.

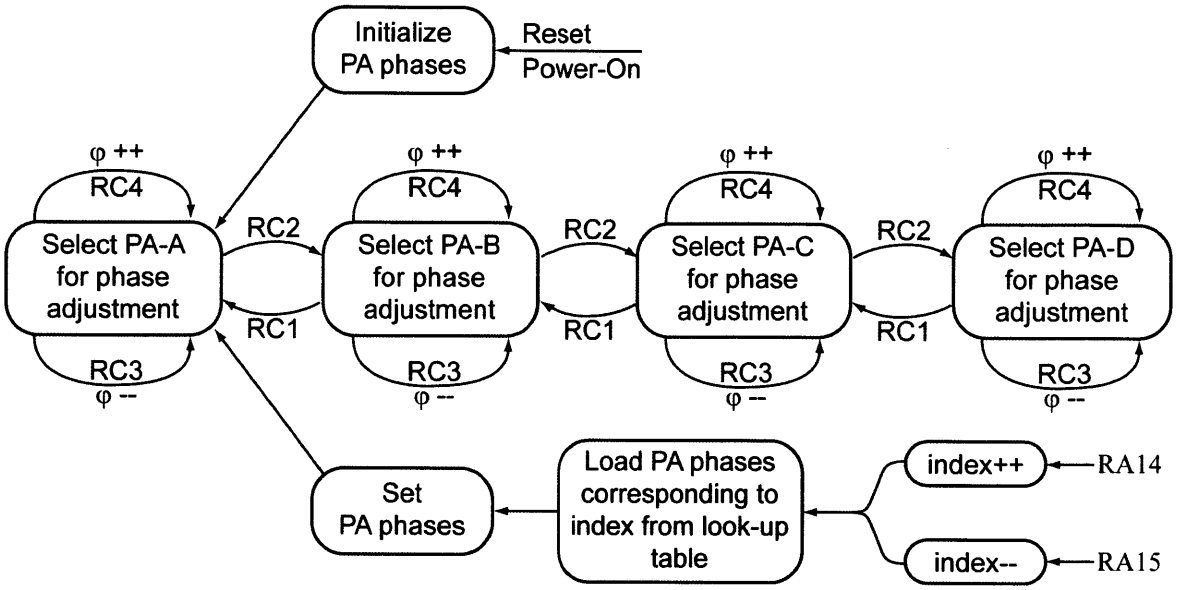



Fig. 3-18: State diagram of the PIC32MX460 firmware developed for controlling the outphasers.

TABLE VII: MAPPING OF THE OUTPHASER BOARD SIGNALS TO THE PINS OF THE MICROCONTROLLER DEVELOPMENT BOARD

| **Outphaser Board Signal** | **Microcontroller Development Board Pin** | | | |
|---|---|---|---|---|
| | **Outphaser A** | **Outphaser B** | **Outphaser C** | **Outphaser D** |
| DA0 | RB0 | RD0 | RE0 | RG6 |
| DA1 | RB1 | RD1 | RE1 | RG7 |
| DA2 | RB2 | RD2 | RE2 | RG8 |
| DA3 | RB3 | RD3 | RE3 | RG9 |
| DA4 | RB4 | RD4 | RE4 | RG12 |
| DA5 | RB5 | RD5 | RE5 | RG13 |
| DA6 | RB6 | RD6 | RE6 | RG14 |
| DA7 | RB7 | RD7 | RE7 | RG15 |
| DA8 | RA0 | RB8 | RD8 | RF0 |
| DA9 | RA1 | RB9 | RD9 | RF1 |
| DA10 | RA2 | RB10 | RD10 | RF2 |
| DA11 | RA3 | RB11 | RD11 | RF3 |
| SELECTIQ | RA4 | RB12 | RD12 | RF8 |
| RESETIQ | RA5 | RB13 | RD13 | RF12 |
| CLKIQ | RA6 | RB14 | RD14 | RF13 |
| WRTIQ | RA7 | RB15 | RD15 | RE9 |

## Chapter 4

# Power Combining System Performance

The previous chapters have described in detail the principles of operation, the design, and the implementation of the proposed power combining and outphasing system. This chapter evaluates the practical performance of the implemented system. First, an empirical port-parameter network model is constructed of the implemented four-way combiner based on various combiner port impedance measurements. This model allows a crude evaluation of the accuracy with which the combiner has been implemented, i.e. how closely do the values of the reactive elements of the built combiner match the intended design values.

The utilized experimental setup is described in detail, and a step-by-step setup procedure is provided. The performance of the combiner is first examined as an independent block and its ability to combine power over its entire operating range while maintaining resistive PA loading is evaluated. Finally, the performance of the entire outphasing and combining system as a whole is discussed.

## 4.1. Combiner Port-Parameter Model

By design, the ideal four-way combiner implementation of Fig. 3-4 has only twelve reactive components. Its "real-world" implementation, however, includes many undesired parasitic reactances such as stray capacitances between the combiner PCB traces and the ground plane, cross-coupling capacitances and mutual inductances between the various combiner branches, PCB trace inductances and resistances, etc. It is valuable to know how closely the actual combiner implementation matches the ideal one, and how the parasitics affect the combiner's performance. Nevertheless, developing a model that takes into account each individual parasitic element is quiet a cumbersome task. Instead, a more "macroscopic" approach is chosen, where the combiner is modeled as a "black-box" with four input ports A-D and a single output port OUT (see Fig. 3-4). In this case, impedance parameters have been selected to describe the relationship between the various terminal voltages and currents at the combiner's ports (59).

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \\ V_{OUT} \end{bmatrix} = \bar{Z}\bar{I} = \begin{bmatrix} z_{11} & z_{12} & z_{13} & z_{14} & z_{15} \\ z_{21} & z_{22} & z_{23} & z_{24} & z_{25} \\ z_{31} & z_{32} & z_{33} & z_{34} & z_{35} \\ z_{41} & z_{42} & z_{43} & z_{44} & z_{45} \\ z_{51} & z_{52} & z_{53} & z_{54} & z_{55} \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \\ I_{OUT} \end{bmatrix} \tag{59}$$

By empirically determining the z-parameters from actual combiner measurements, one can develop a relatively accurate model of the real combiner which incorporates the effect of the various parasitic elements and mismatches in the combiner branch reactances. Although this model does not offer significant insight in the nature of the parasitics or branch reactance mismatches, it allows one to examine their effect on the combiner's key characteristics. The z-parameters can be easily calculated from a set of impedance measurements performed on the combiner's ports. Matrix M (60) is the result of performing such measurements on the implemented combiner PCB. The diagonal entries of M ($m_A$-$m_{OUT}$) correspond to the impedance seen at the corresponding combiner port with all other ports left open, e.g. $m_A$ is the impedance seen looking into port A with ports B, C, D, and OUT left open. On the other hand, matrix entries $m_{I,J}$ correspond to the input impedance measured at port I, with port J shorted, and all other ports open. All impedance measurements are performed at 27.12 MHz using an impedance analyzer (4395A, Agilent Technologies Inc.). Shorted ports are terminated with a short-circuit stub (PE6006, Pasternack).

$$M = \begin{bmatrix} m_A & m_{A,B} & m_{A,C} & m_{A,D} & m_{A,OUT} \\ m_{B,A} & m_B & m_{B,C} & m_{B,D} & m_{B,OUT} \\ m_{C,A} & m_{C,B} & m_C & m_{C,D} & m_{C,OUT} \\ m_{D,A} & m_{D,B} & m_{D,C} & m_D & m_{D,OUT} \\ m_{OUT,A} & m_{OUT,B} & m_{OUT,C} & m_{OUT,D} & m_{OUT} \end{bmatrix}$$

$$M = \begin{bmatrix} 96.5-308j & 2.18+0.887j & 4.43-76.8j & 4.23+1.49j & 3.62-87.2j \\ 1.72+0.740j & 87.8-246j & 3.24-2.91j & 6.47+78.0j & 1.94-13.7j \\ 3.88-70.0j & 3.49-3.36j & 86.7-280j & 2.38+3.41j & 2.21+12.5j \\ 3.01+1.16j & 5.42+70.2j & 1.76+2.75j & 79.7-220j & 4.68+86.6j \\ 4.45-74.3j & 1.70-14.4j & 1.82+11.7j & 8.24+100j & 85.9-260j \end{bmatrix} \quad (59)$$

Note that the diagonal elements of Z (58) correspond directly to the diagonal elements of M, as both set of elements reflect the input port impedance of a particular combiner port with all other ports open-circuited, i.e. $z_{11} = m_A$, $z_{22} = m_B$, etc. Once the diagonal elements of Z are known, the rest of the elements can be easily computed. For example, consider measuring the input port impedance at port A, while port B is shorted (all other ports are open-circuited). Then from (58):

$$\begin{aligned} V_A &= z_{11}I_A + z_{12}I_B \\ V_B &= z_{21}I_A + z_{22}I_B = 0 \end{aligned} \quad (60)$$

Also, note that as already mentioned $z_{11} = m_A$ and $z_{22} = m_B$. Moreover, since the combiner comprises only linear passive elements, it is reciprocal and its impedance matrix Z is symmetric, and so $z_{12} = z_{21}$. Since $V_A/I_A = m_{A,B}$ for $V_B = 0$ and ports C, D, and OUT open-circuited, it can be shown from (60) that $z_{12} = z_{21}$ is given by (61).

$$z_{12} = z_{21} = \sqrt{(m_A - m_{A,B})m_B} \tag{61}$$

The rest of the z-parameters can be determined by applying an analogous approach. The full Z matrix is given in (62).

$$Z = \begin{bmatrix} 96.5-309j & 91.2-276j & 90.0-255j & 86.1-262j & 89.9-240j \\ 91.2-276j & 87.8-246j & 85.7-261j & 81.7-268j & 86.0-250j \\ 90.0-255j & 85.7-261j & 86.7-281j & 82.3-250j & 85.4-276j \\ 86.1-262j & 81.7-268j & 82.3-250j & 79.7-220j & 81.1-283j \\ 89.9-240j & 86.0-250j & 85.4-276j & 81.1-283j & 85.9-260j \end{bmatrix} \tag{62}$$

Suppose that the combiner's output port is now loaded resistively with 50 Ω, i.e. $V_{OUT}/I_{OUT}$ = 50 Ω. By imposing such a relationship between $V_{OUT}$ and $I_{OUT}$, and employing (59), one can obtain the effective input admittance matrix of the implemented combiner. This matrix is analogous to the one derived for the ideal four-way combiner of Fig. 2-5 (16). As it is based on actual port-parameter measurements, one can regard it as crude model of the implemented combiner. Thus, it can be used to compute approximately the expected input admittance and output power characteristics of the implemented combiner. By comparing these characteristics to those of the ideal combiner, one can appreciate how closely the combiner implementation agrees (in terms of mismatch between the reactive elements and the presence of parasitics) with the ideal combiner design. Fig. 4-1 and Fig. 4-2 illustrate respectively the output power and input admittance characteristics of the ideal and implemented combiners (see Appendix C, port_param_compare.m for a MATLAB script).

The commanded power is the combiner output power that one desires to achieve (the power based on which the outphasing control angles are selected). As expected, in the case of the ideal combiner, the output power is equivalent to the commanded power. Moreover, it can be seen from Fig. 4-1 that for the same ideal outphasing control angles, the expected output power of the implemented combiner closely matches that of the ideal one.

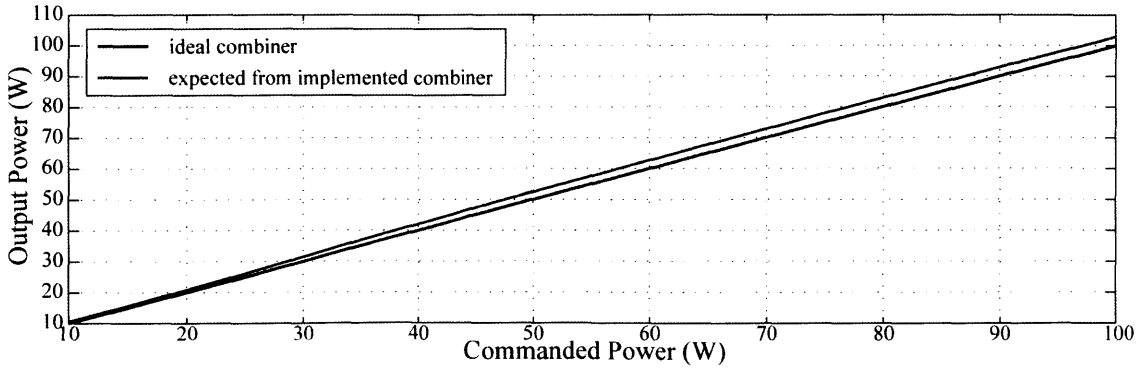



Fig. 4-1: Comparison between the expected output power from the implemented and ideal combiners versus commanded power.

Furthermore, as can be seen from Fig. 4-2 (top), the expected effective input conductances of the implemented combiner are in good agreement with those of the ideal combiner. Although the expected input susceptance characteristic (Fig. 4-2, bottom) deviates appreciably from the ideal one, the overall input admittance remains predominantly resistive, especially at higher output power levels.

Nevertheless, it is interesting to examine the extent to which the input admittance characteristic of the implemented combiner can be corrected (altered to match better the ideal characteristic) by just tweaking the outphasing control angles. Performing a numerical optimization on the outphasing control angles to minimize the expected input susceptance of the implemented combiner over its operating power range reveals the optimum input admittance characteristic shown in Fig. 4-3 (see Appendix C, port_param_compare.m for a MATLAB script). Although the resultant peak loading susceptance is reduced to approximately 4 mS, the susceptance characteristic is still appreciably different from the ideal one. Based on the measured port-parameters of the implemented combiner, the susceptance characteristic of Fig. 4-3 is the most optimal one that can be achieved based on outphasing angle correction alone. A comparison between the ideal outphasing control angles $\theta$ and $\phi$, and the optimized ones is shown in Fig. 4-4. This suggests that even though one can tweak slightly the control angles to account for mismatches in the combiner's reactances and its parasitics (to a somewhat limited extent), in order to obtain combiner behavior close to that of the ideal one, it is crucial to accurately tune its reactive elements and minimize parasitics.

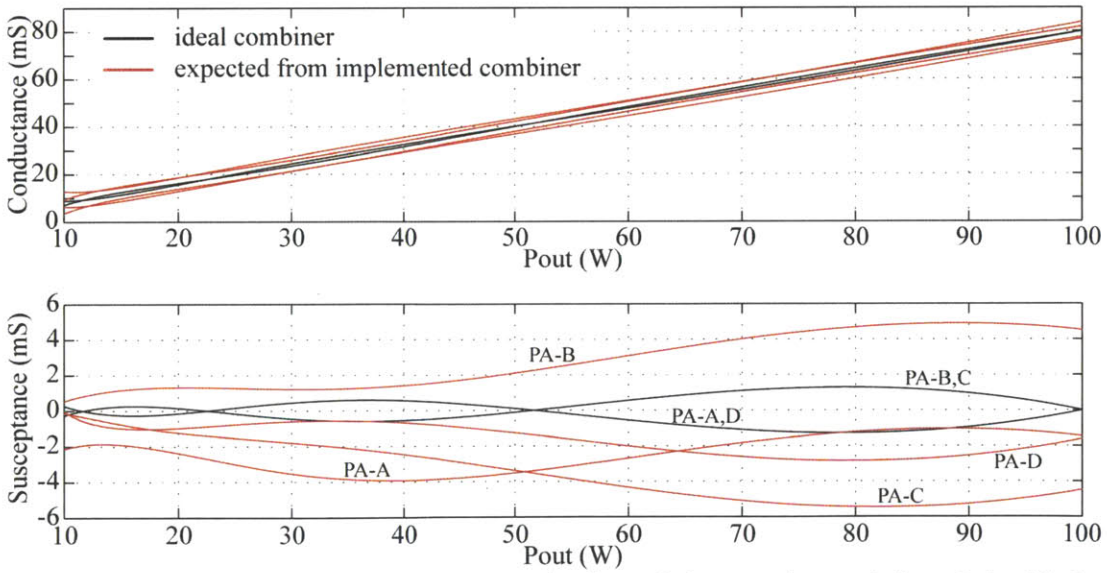



Fig. 4-2: Comparison between the expected PA loading admittance characteristics of the ideal and implemented combiners versus output power.

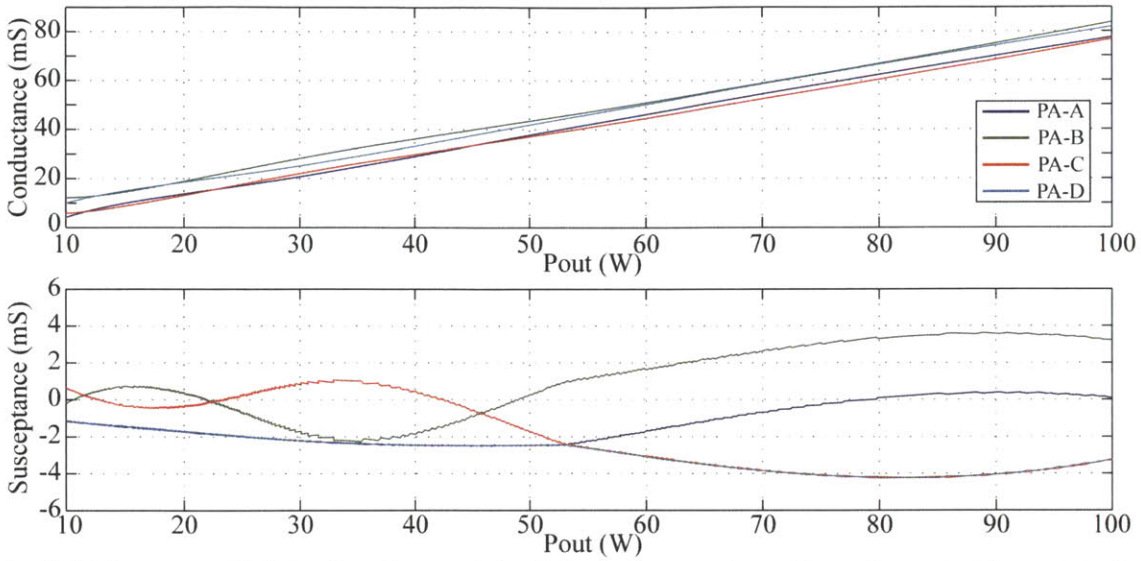



Fig. 4-3: The expected PA loading characteristic of the implemented combiner after optimizing outphasing control angles based on the measured port-parameter combiner model.

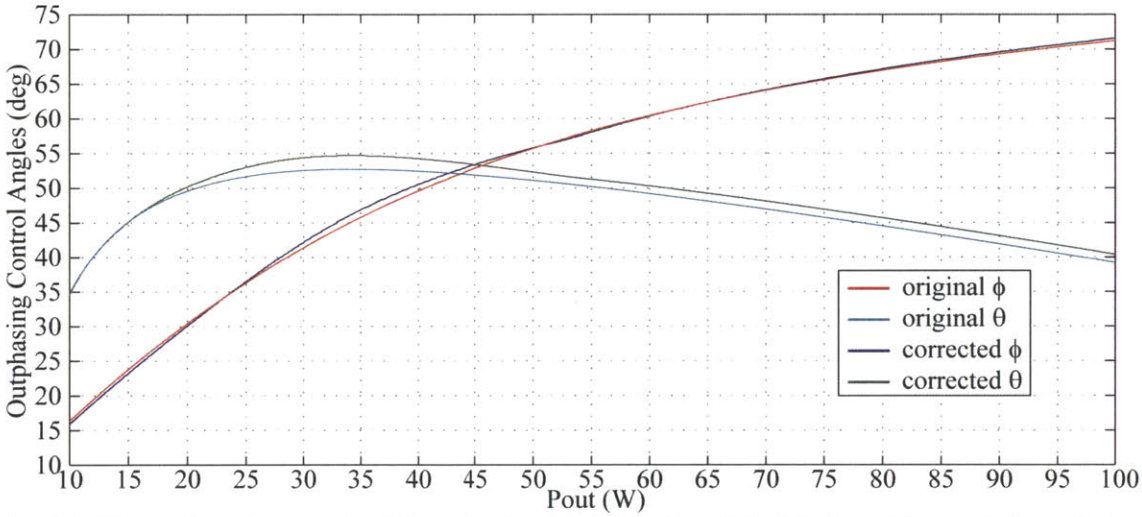



Fig. 4-4: Comparison between the OS outphasing control angles of the ideal combiner and the optimized OS control angles for the implemented combiner.

## 4.2. Experimental System Setup

This section describes the experimental setup and provides a detailed step-by-step procedure for setting-up the entire system and preparing it for performing the necessary performance measurements. A block diagram of the overall power combining and outphasing system is shown in Fig. 4-3.

The PIC32MX460F microcontroller is programmed with the developed system control firmware (Appendix E), and the development board is connected to the four outphaser PCBs via a set of ribbon cables as per the pin mapping given in Table VII. All outphaser PCBs share the same reference LO signal - a 27.12 MHz, 5 $V_{pp}$ sinusoidal wave. The outphaser's outputs (OUT1, Fig. 3-15) connect respectively to the

input ports of the PAs via 50 Ω coaxial cables. Although in the present setup these coaxial cables have nearly identical electrical length, this is not a crucial requirement. The developed microcontroller firmware allows one to calibrate-out any undesired delays in the signal path through independent (and manual) adjustment of each of the outphasing angles. The PAs are powered from a nominal +16V supply. Pair-twisted 16AWG wires with 10 turns on a ferrite core (28B2000-100, Laird-Signal Integrity Products) are used to connect the PA drain supply to the PA PCB power connector (SL1, PA schematic, Appendix D.3). Four SMA-to-SMA (72964, Pomona Electronics) plugs connect each of the PA's outputs to the combiner's respective input power ports.

Four 10 MΩ, 8 pF oscilloscope probes (P6139A, Tektronix Inc.) are connected respectively to test points TP1-TP4 (see Fig. 3-5) to monitor the input voltage waveforms at the combiner's input ports and ensure correct inputs signal phases (within ±1°) and fundamental harmonic amplitudes. A 100 W, 30 dB attenuator (Part #: 690-30-1, Meca Electronics Inc.) loaded with the input channel of an oscilloscope (TDS3014B, Tektronix Inc.), set to 50Ω input impedance, is employed as a load for the combiner. The VSWR, as seen by the combiner's output port, is measured to be approximately 1.04. The combiner output power is measured using a directional RF power meter (5010B, Bird Electronics Corp.). Fig. 4-5 shows photograph of the entire experimental setup.

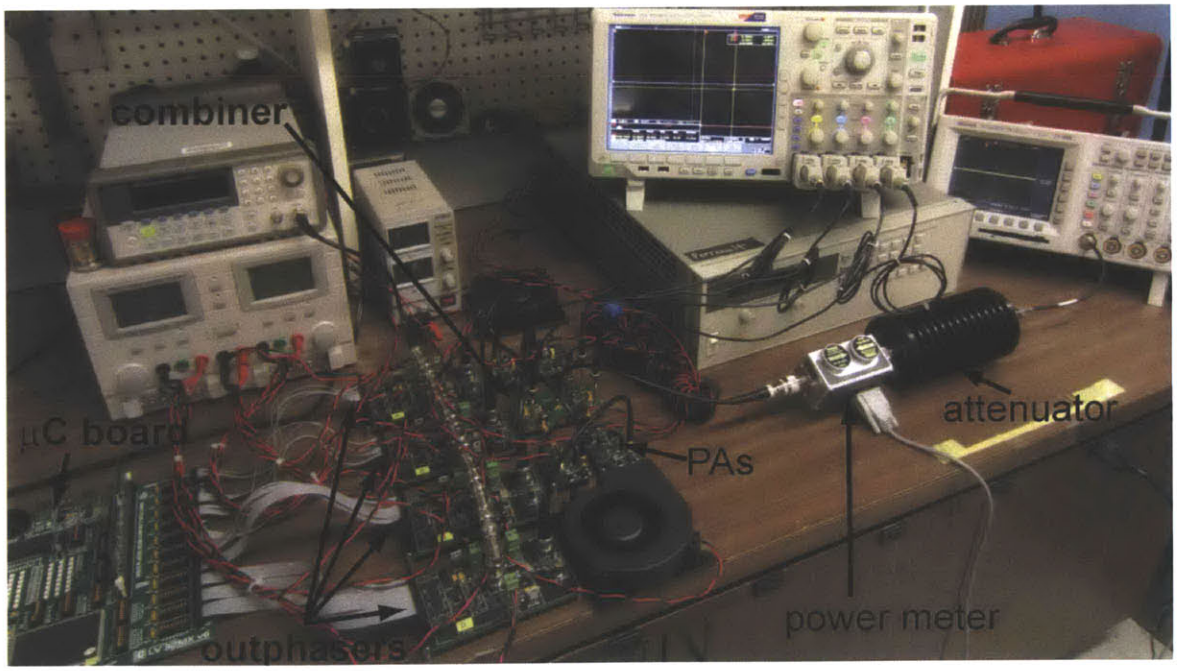



Fig. 4-5: Photograph of the experimental setup.

The procedure provided assumes that all the individual system blocks are fully assembled and operational.

System Set-Up Procedure:

1. Program the microcontroller with the system control firmware (Appendix E).
2. Connect each of the four outphaser PCBs (A-D) with a ribbon cable to its corresponding connection terminal on the development board as per Table VII.
3. Connect each of the supply terminals (+3V3, +5V, +12V) on the outphaser PCBs to the indicated below DC power supply voltage levels. Do not power up the outphaser PCBs at this point.

   +3V3 → VDC > 3.5V

   +5V → VDC > 5.5V

   +12V → VDC > 12.5V
4. Connect all of the outphaser's LO reference oscillator input ports via a 50 Ω coaxial cable to the same output port of a waveform generator capable of generating a 27.12 MHz, 5 $V_{pp}$ sinusoidal signal into a 50 Ω load.
5. Connect the input port (Fig. 3-11, IN) of each of the four PAs (A-D) to the output port (Fig. 3-15, OUT1) of a corresponding outphaser (A-D) using 50 Ω BNC-to-SMA coaxial cables having equal electrical lengths.
6. Connect the PA's output ports (Fig. 3-11, OUT) to the combiner's input power ports (A-D) using an SMA (male)-to-SMA (male) plug (72964, Pomona Electronics).
7. Connect each of the PA logic circuit supply terminals (SL2, PA schematic, Appendix D.3) to +5V supply. Do not power-up the PA logic circuitry at this point.
8. Connect each of the PA drain supply terminals (SL1, Appendix schematic) to +16V supply through a 16AWG wire with 10 turns on a ferrite core (such as 28B2000-100, Laird-Signal Integrity Products). Do not power-up the PA at this point.
9. Connect the combiner's output power port (Fig. 3-5, OUT) to the input port of an oscilloscope (TDS3014B, Tektronix Inc.) through a power meter sensor (5010B, Bird Electronics Corp.) and a 100W, 30 dB attenuator (Part #: 690-30-1, Meca Electronics Inc.). Set the oscilloscope port input impedance to 50 Ω.
10. Connect the four oscilloscope probes (P6139A, Tektronix Inc.) to the four combiner test-points (Fig. 3-5, TP1-4).

System Power-Up Procedure:

11. Power-up the microcontroller and the development board. Restart the microcontroller (RESET push-button on the development board)
12. Power-up the LO waveform generator and set it to generate a 27.12 MHz, 5 Vpp sinusoidal voltage signal into a 50 Ω load impedance.

13. Power-up the outphaser PCB supplies (+3V3, +5V, +12V). If the outphasers are powered correctly, a green LED lights-up next to each supply terminal connector.
14. Restart the microcontroller (RESET push-button on the development board).
15. Power-up the PA logic circuitry.
16. Power-up the PA drain supply.
17. The system is operational. The development board can be used to outphase the PAs as per Section 3.5.

## 4.3. Combiner Performance

In order to evaluate the performance of the power combiner and asses the validity of the proposed outphasing control law, the system is tested at various output power levels over approximately a 10 dB power range ratio. For a given desired output power (termed here "commanded" power) the PAs are outphased according to Fig. 2-4, with $\theta$ and $\phi$ selected for the corresponding power level from Fig. 2-9. Moreover, the PA's DC supply voltages are appropriately adjusted over the combiner's operating range to ensure that the amplitude of the fundamental component of their output voltage waveforms is always maintained at approximately 25 V for all output power levels (consistent with Fig. 2-4). Effectively, this results in driving the combiner with zero-output impedance PAs (similar to treating the PAs as ideal voltage sources). It is well recognized that this method for driving the combiner does not accurately reflect the constraints of a "real-life" application; modulation of the PA's DC supply voltage is not a luxury that one can afford in an actual power combining system. Nevertheless, it is important to clarify that the sole purpose of the system implementation discussed above is to allow for an experimental verification of the power combiner's combining characteristics and evaluation of the effectiveness of the proposed outphasing law to control output power. The performance of the entire power combining system as a whole is discussed in the following subsection.

The relationship between the measured combiner output power and commanded power is plotted in Fig. 4-6. Ideally the output power should be equivalent to the commanded power (indicated with a dashed line in Fig. 4-6). The close agreement between the actual output power and ideal output power is evident. This demonstrates that the proposed outphasing control law can be effectively utilized in controlling the output power delivered to a load.

It is also of interest to examine the efficiency of the entire combining and outphasing system. Here, system efficiency is determined by the ratio of output power delivered to the load to the total PA DC drain input power (i.e. excluding PA gate-driving power). Fig. 4-7 shows the measured system efficiency over a 10 dB output power range (plotted in red) with the error bars representing a ±5% measurement error of the power meter measurements. The measured average PA efficiency curve (shown in blue) is obtained by first measuring independently, and then averaging the efficiencies of each of the four PAs loaded resistively over a range of output power levels, while maintaining a 25 V constant-amplitude fundamental frequency

component of the PA output voltages. These efficiency measurements are consistent with the combiner driving methodology described earlier.

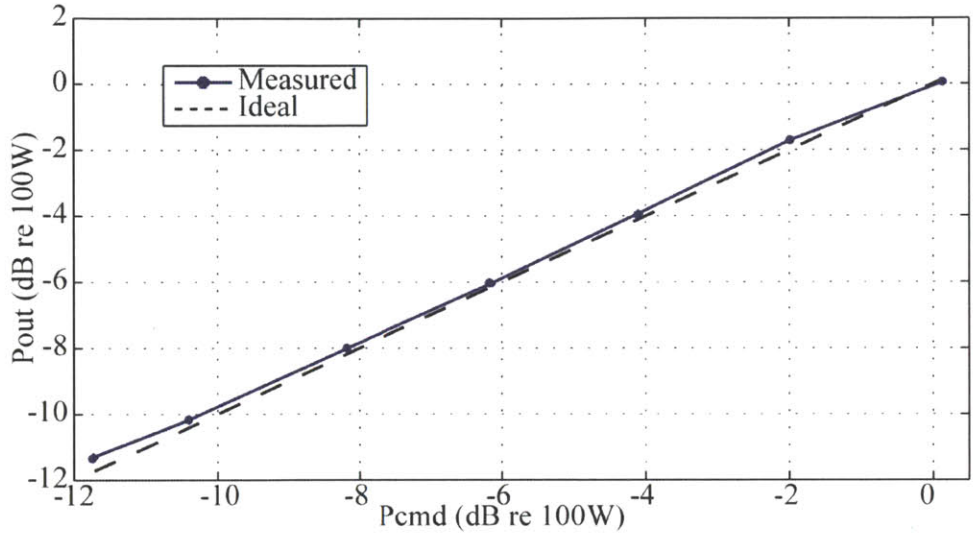



Fig. 4-6: Measured combiner output power $P_{out}$ versus commanded output power $P_{cmd}$.

As can be seen from Fig. 4-7, the overall system efficiency is dominated by the PA losses. As it was earlier mentioned, variations in susceptive loading of the PAs (due to any susceptive components of the combiner's effective input admittances) can considerably mistune the output resonant tank of the PAs and introduce additional losses (termed here combiner/PA interface losses). Neglecting such interface losses, one would expect the overall system efficiency to be determined by the product of the PA and power combiner efficiencies. Fig. 4-7 shows the expected system efficiency for the present system (ignoring combiner/PA interface losses) obtained by multiplying the measured average PA efficiency with the combiner efficiency of Fig. 3-6. As can be seen, the expected system efficiency is within the uncertainty of the overall system efficiency measurements, suggesting that indeed, the combiner does maintain an overall resistive loading of the PAs over most of the operating power range.

Fig. 4-8 further shows the distribution of total PA input power among the individual PAs. As can be seen, the employed outphasing control law results in a relatively even loading of the PAs over most of the considered operating range.

## 4.4. Overall System Performance

Similarly to the approach adopted for evaluating the performance of the combiner as an independent block (Section 4.3), the overall system is tested at several output power levels over its intended 10 dB operating range (10 W - 100 W). As already described above, for a given desired output power (termed here "commanded" power) the PAs are outphased according to Fig. 2-4, with $\theta$ and $\phi$ selected for the corresponding power level from Fig. 2-9. The essential difference in evaluating the performance of the overall system in contrast to that of the combiner alone is that the PA drain supply powering all four PAs is

now fixed to 16 V. This reflects accurately the operating conditions in a "real-word" power amplification system where efficient and dynamic PA drain-modulation is hard to achieve, and is usually avoided.

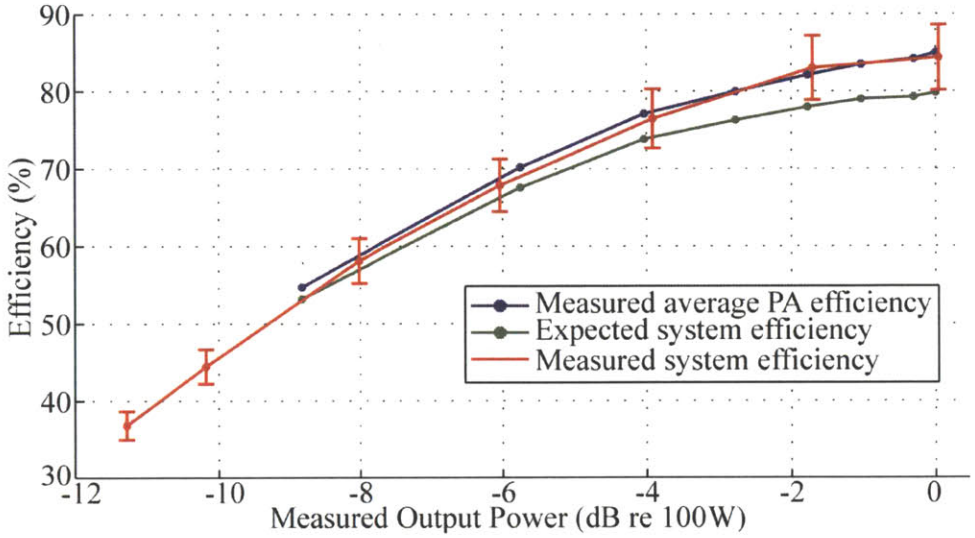



Fig. 4-7: Measured overall system and PA efficiency versus combiner output power.

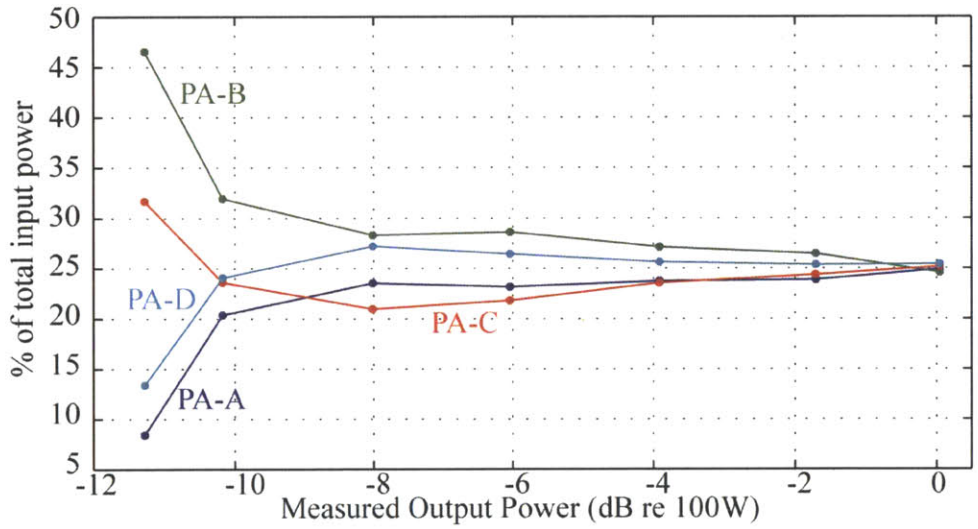



Fig. 4-8: Total input power distribution among PAs versus combiner output power.

As can be seen from Fig. 4-9, the fundamental component (at 27.12 MHz) amplitude of the PA's output decreases with increasing combiner (and PA) output power. This is a clear manifestation of the finite, but non-zero PA output impedance. Furthermore, the loading that the combiner presents to each PA remains approximately evenly distributed among the four PAs as output power is modulated from 10 W to 100 W. This can be inferred from Fig. 4-9 by noting that the PA output amplitude-power characteristic is approximately equivalent for all four PAs.

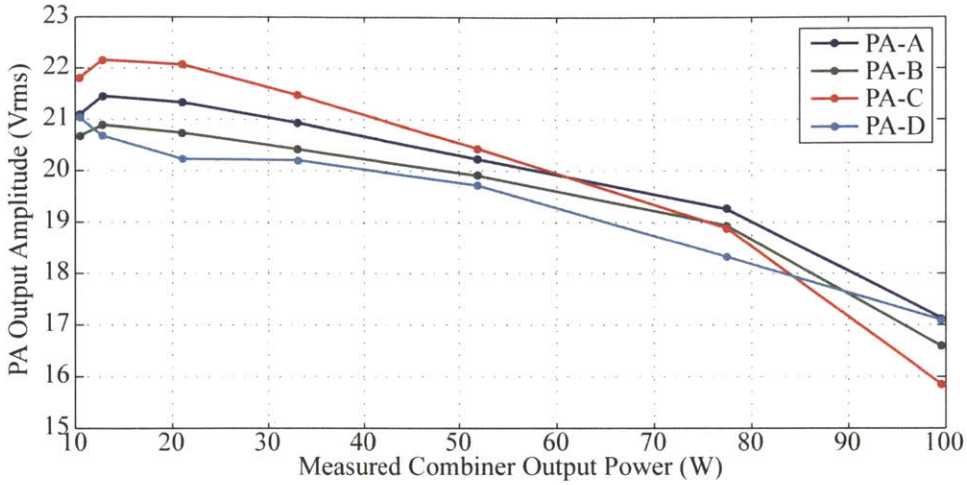



Fig. 4-9: The magnitude of the fundamental component of each of the PA's output voltage waveforms versus combiner output power.

The relationship between the combiner's output power and the commanded power is plotted in Fig. 4-10. It is important to describe the exact steps involved in obtaining the commanded-output power characteristic. In this case, the sets of PA outphasing angles used are identical to the ones used for testing the performance of the combiner as an independent block (Section 4.3). For each set of outphasing angles, the resulting combiner output power and PA output amplitudes (plotted in Fig. 4-9) are measured. A simulation is then performed on the ideal combiner with its input power ports driven with signals having exactly the same amplitudes as the one measured from the real system. The combiner output power predicted from this simulation is effectively the commanded power. It is this commanded power that is compared in Fig. 4-10 to the combiner measured output power, and as can be seen, the two are in reasonable agreement over the entire operating range. In effect, this method is equivalent to pre-distorting the PA outphasing control for a particularly desired output power level in order to compensate for the non-zero PA output impedance and the resulting variation in the PA output amplitudes.

To achieve an accurate control of the system's output power in spite of the various non-idealities in the implemented system (such as non-zero PA output impedance, mismatches in the combiner reactances, parasitics, etc.), one usually must determine empirically the mapping between the outphasing angles and the output power. This approach is often employed with the control of various non-linear systems.

It is also of interest to examine the efficiency of the entire combining and outphasing system. Here, system efficiency is determined by the ratio of output power delivered to the load to the total PA DC drain input power (i.e. excluding PA gate-driving power). Fig. 4-11 shows the measured system efficiency over a 10 dB output power range (plotted in red) with the error bars representing a ±5% measurement error of the power meter measurements. The measured average PA efficiency curve (shown in blue) is identical to the one depicted in Fig. 4-7.

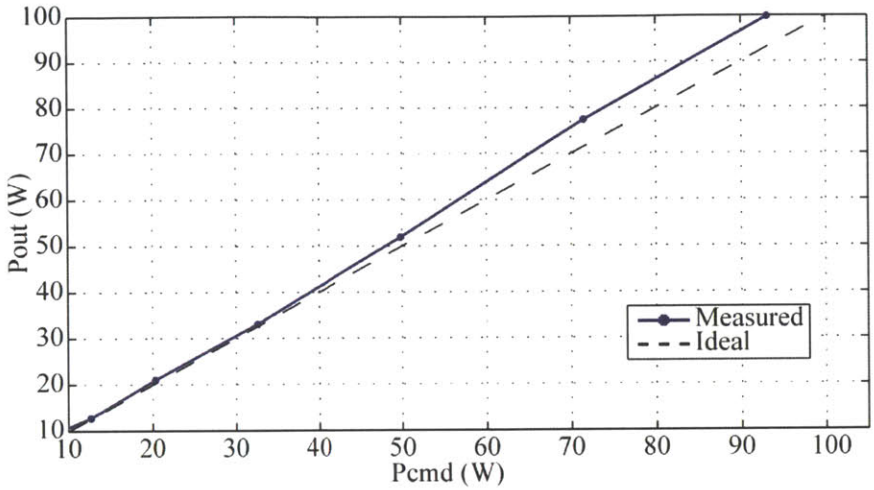



Fig. 4-10: Measured combiner output power $P_{out}$ versus commanded power $P_{cmd}$.

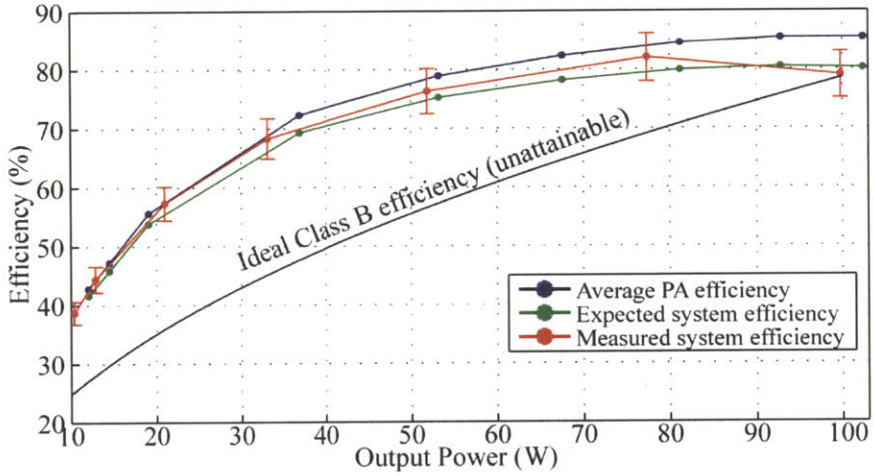



Fig. 4-11: Comparison between measured system power efficiency, expected system efficiency, average PA efficiency, and the efficiency that can be expected from a similar system if it were implemented with an ideal linear class-B PA.

As can be seen from Fig. 4-11, similarly to Fig. 4-7, the overall system efficiency is dominated by the PA losses. Moreover, the expected system efficiency (identical to the one shown in Fig. 4-7) is within the uncertainty of the overall system efficiency measurements, suggesting that indeed, the combiner does maintain an overall resistive loading of the PAs over most of the operating power range even with PA output amplitude modulation.

For the sake of comparison, Fig. 4-11 illustrates the overall system efficiency one would expect to achieve from a power combining system implemented with an ideal class-B linear amplifier. (At its peak output power, an ideal class-B amplifier has an efficiency of $\pi/4$ or 78.5 %.) Clearly, the presently implemented power combining system incorporating power combing from non-linear amplifiers exhibits dramatic efficiency improvements compared to its class-B counterpart, not to mention that the class-B efficiency curve shown in Fig. 4-11 is unattainable in reality.

## Chapter 5

# Power Combiner Adaptation for High-Frequency Applications

This thesis has so far considered only the design and implementation of a lumped-element combiner. Although a lumped-element approach is a reasonable choice at 27.12 MHz, for applications involving much higher operating frequencies (in the GHz range) where the wavelength is comparable to the combiner's physical size, one must take into account the transmission-line effects. Furthermore, at sufficiently high frequencies the quality of discrete passive components (such as capacitors and inductors) can significantly degrade, and accuracy and repeatability of component values and accuracy of component placement become challenging issues. To address these issues, a transmission-line implementation of a multi-way lossless outphasing combiner is proposed, which allows one to realize an outphasing architecture and operating characteristics similar to those described above using only transmission lines. Asymmetric transmission-line-only power combiners have been previously proposed in place of Chireix power combiners for two-way outphasing systems [51, 63]; here we develop transmission-line-only combining for multi-way lossless outphasing. Such a transmission-line implementation greatly simplifies the construction of the combiner as the transmission lines can be laid out directly on a printed circuit board (PCB). This chapter discusses one possible transmission-line implementation of the proposed combiner, presents its combining characteristics, and outlines a design methodology.

## 5.1. Transmission-Line Implementation

One possible transmission-line (TL) implementation of the four-way combiner of Fig. 2-5 is shown in Fig. 5-1, with each of the $X_1$ and $X_2$ combiner reactances replaced respectively with transmission lines with impedances $Z_1$ and $Z_2$. Each of the transmission lines has a half-wavelength base length, i.e. their lengths are defined as a particular increment/decrement $\Delta L_1$ and $\Delta L_2$ from a half-wavelength transmission line. This methodology for sizing the transmission lines allows for design symmetry and greatly simplifies the analysis of the combiner. Although other base-length choices are possible, a half-wavelength is the shortest possible TL length that will allow for symmetric length increments $\pm\Delta L_{1,2}$. Half wavelength increments may be added to the base transmission line lengths without changing the operating characteristics, but shorter lengths are preferable when possible because of practical loss considerations. The design methodology for selecting the TL impedances $Z_1$ and $Z_2$ and their respective length increments $\Delta L_1$, $\Delta L_2$ is described in Subsection 5.5. Note that although the combiner network is designed for a particular load resistance $R_L$, its output may be terminated with an impedance transformation stage (such as matching

network, or transmission-line transformer) that converts the actual load impedance $R_{L0}$ to the impedance $R_L$ for which the combiner is designed (see Fig. 5-1). Such impedance transformation introduces greater design flexibility and allows one to design the combiner network without the necessity for transmission lines with high characteristic impedances.

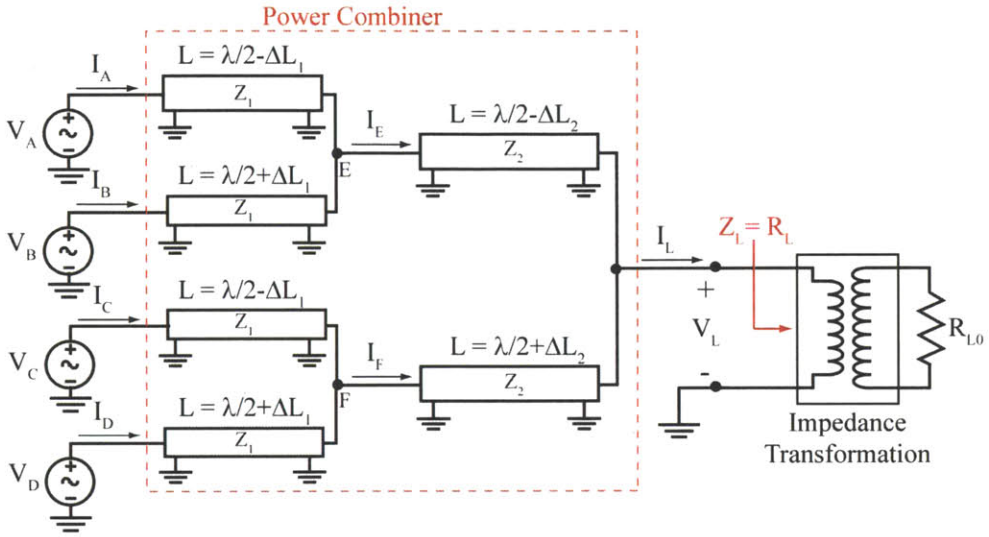



Fig. 5-1: Transmission-line implementation of the four-way combiner of Fig. 2-5 using transmission lines with characteristic impedance of $Z_1$ and $Z_2$. The lengths of the transmission lines are defined as $\pm\Delta L_1$ and $\pm\Delta L_2$ increments to a half-wavelength base length.

## 5.2. Input-Port Admittance Characteristics

Understanding of the effective input admittance characteristics of the TL combiner of Fig. 5-1 is important for its design and analysis. A convenient approach for determining these characteristics is to first derive an effective admittance matrix similar to the one described in Section 2.3 (16), relating the input port currents $I_A$-$I_D$ to its input terminal voltages $V_A$-$V_D$. Based on this matrix, one can then easily compute the input admittance (effective PA loading) of any input port of the combine for any arbitrary outphasing control methodology.

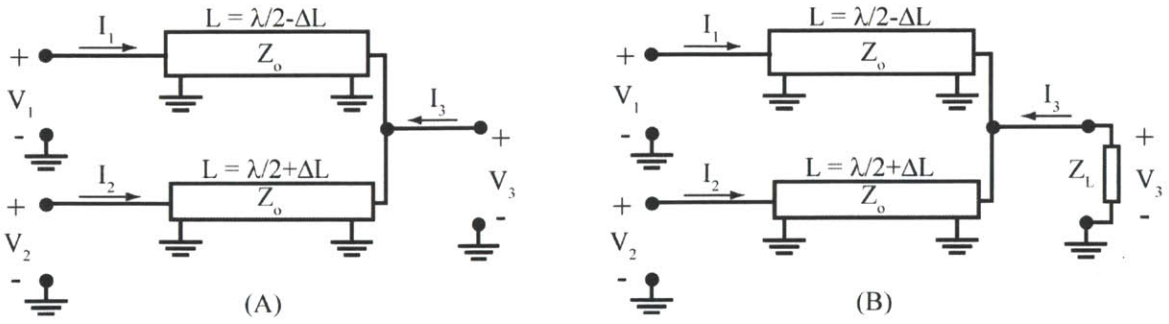



Fig. 5-2: Transmission-line networks for deriving the effective input admittance matrix of the TL combiner of Fig. 5-1.

To derive the admittance matrix of the TL combiner, consider the three-port network of Fig. 5-2(A). Conventional transmission-line analysis methods can be employed to show that its terminal voltages and input-port currents are related according to (63), where $\sigma = 2\pi\Delta L/\lambda$. Furthermore, by loading port 3 with an arbitrary impedance $Z_L$ and demanding that $V_3/I_3 = -Z_L$, one can show that (64) describes the relationship between the terminal voltages and input currents of the network in Fig. 5-2(B).

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \frac{j}{Z_o \, sin(\sigma)} \begin{bmatrix} -cos(\sigma) & 0 & -1 \\ 0 & cos(\sigma) & 1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{63}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{Z_L}{Z_o^2 \, sin^2(\sigma)} \begin{bmatrix} 1 - j\frac{Z_o}{Z_L} cos(\sigma) sin(\sigma) & -1 \\ -1 & 1 + j\frac{Z_o}{Z_L} cos(\sigma) sin(\sigma) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{64}$$

Referring to Fig. 5-1, and employing the admittance matrices given by (62) and (63), the various branch currents $I_A$-$I_F$, and node voltages $V_A$-$V_F$ can be related according to (65).

$$\begin{bmatrix} I_A \\ I_B \\ I_E \end{bmatrix} = \frac{j}{Z_1 \, sin(\sigma_1)} \begin{bmatrix} -cos(\sigma_1) & 0 & -1 \\ 0 & cos(\sigma_1) & 1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_E \end{bmatrix} \tag{65a}$$

$$\begin{bmatrix} I_C \\ I_D \\ I_F \end{bmatrix} = \frac{j}{Z_1 \, sin(\sigma_1)} \begin{bmatrix} -cos(\sigma_1) & 0 & -1 \\ 0 & cos(\sigma_1) & 1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_C \\ V_D \\ V_F \end{bmatrix} \tag{65b}$$

$$\begin{bmatrix} I_E \\ I_F \end{bmatrix} = \frac{R_L}{Z_2^2 \, sin^2(\sigma_2)} \begin{bmatrix} 1 - j\frac{Z_2}{R_L} cos(\sigma_2) sin(\sigma_2) & -1 \\ -1 & 1 + j\frac{Z_2}{R_L} cos(\sigma_2) sin(\sigma_2) \end{bmatrix} \begin{bmatrix} V_E \\ V_F \end{bmatrix} \tag{65c}$$

By solving (65) for the combiner input-port currents $I_A$-$I_D$ as a function of its terminal voltages $V_A$-$V_D$, one can obtain the TL combiner admittance matrix (66), where sub-matrices $M_1$, $M_2$ and $M_3$ are respectively given by (67)-(69).

$$\begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \end{bmatrix} = Y_{eff} \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = \begin{bmatrix} M_1 & M_2 \\ M_2 & M_3 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} \tag{66}$$

$$M_1 = \begin{bmatrix} \gamma sec^2(\sigma_2) + j(cos(\sigma_1)sin(\sigma_1) - \beta tan(\sigma_2)) & -\gamma sec^2(\sigma_2) + j\beta tan(\sigma_2) \\ -\gamma sec^2(\sigma_2) + j\beta tan(\sigma_2) & \gamma sec^2(\sigma_2) - j(cos(\sigma_1)sin(\sigma_1) + \beta tan(\sigma_2)) \end{bmatrix} \quad (67)$$

$$M_3 = \begin{bmatrix} \gamma sec^2(\sigma_2) + j(cos(\sigma_1)sin(\sigma_1) + \beta tan(\sigma_2)) & -\gamma sec^2(\sigma_2) - j\beta tan(\sigma_2) \\ -\gamma sec^2(\sigma_2) - j\beta tan(\sigma_2) & \gamma sec^2(\sigma_2) - j(cos(\sigma_1)sin(\sigma_1) - \beta tan(\sigma_2)) \end{bmatrix} \quad (68)$$

$$M_2 = \begin{bmatrix} \gamma sec^2(\sigma_2) & -\gamma sec^2(\sigma_2) \\ -\gamma sec^2(\sigma_2) & \gamma sec^2(\sigma_2) \end{bmatrix} \quad (69)$$

Furthermore, if one assumes that the PAs driving the TL combiner are outphased according to Fig. 5-3 (also see Fig. 2-4) with the combiner terminal voltages $V_A$-$V_D$ given by (17) (and repeated below for convenience), then (66) can be solved to yield the effective combiner input admittances $Y_{eff,A}$-$Y_{eff,D}$ in terms of the outphasing angles $\theta$ and $\phi$:

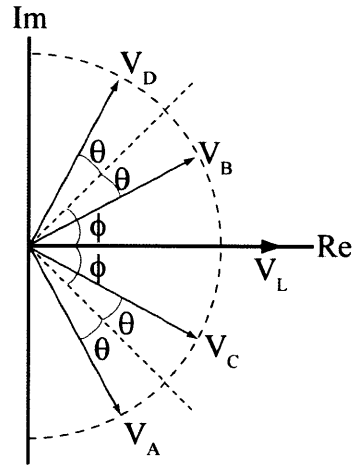



Fig. 5-3: Phasor representation of the output voltages $V_A$-$V_D$ of the PAs driving the combiner of Fig. 5-1.

$$\vec{V} = \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{+j\phi}e^{-j\theta} \\ e^{-j\phi}e^{+j\theta} \\ e^{+j\phi}e^{+j\theta} \end{bmatrix} \quad (17)$$

As with to the lumped combiner implementation, it can be seen from (70) that the input admittances at ports A/D and B/C are complex conjugate pairs. It is interesting to note that if the transmission line impedances $Z_1$ and $Z_2$ are selected to be respectively $X_1/\sin(\sigma_1)$ and $X_2/\sin(\sigma_2)$, where $X_1$ and $X_2$ are the branch reactances of the lumped combiner of Fig. 2-5, then in the limit of $\sigma_1$ and $\sigma_2$ being zero, (66)-(70) become identical to (16) and (18)-(21). In other words, by making $\sigma_1$ and $\sigma_2$ sufficiently small, and choosing $Z_1=X_1/\sin(\sigma_1)$ and $Z_2=X_2/\sin(\sigma_2)$, one can design the TL combiner to approximately match the behavior of the lumped combiner. Of course, there is a practical limit to how small one can pick $\sigma_1$ and $\sigma_2$ to be, as too small values result in extremely large transmission-line impedances which are hard to realize.

$$Y_{eff,A} = \frac{csc^2(\sigma_1)sec^2(\sigma_2)}{Z_1}\left[sin(\phi)(-\beta cos(\phi)sin(2\sigma_2) + 4\gamma cos(\theta)sin(\theta+\phi))\right. \\ \left. + j(cos(\sigma_1)cos^2(\sigma_2)sin(\sigma_1) + sin^2(\phi)(2\gamma sin(2\theta) - \beta sin(2\sigma_2)) - 2\gamma cos^2(\theta)sin(2\phi))\right] \quad (70a)$$

$$Y_{eff,B} = \frac{csc^2(\sigma_1)sec^2(\sigma_2)}{Z_1}\left[2sin(\phi)(-2\gamma cos(\theta)sin(\theta-\phi) + \beta cos(\phi)sin(\sigma_2)cos(\sigma_2))\right. \\ \left. - j(cos(\sigma_1)cos^2(\sigma_2)sin(\sigma_1) + sin(\phi)(-4\gamma cos(\theta)cos(\theta-\phi) + \beta sin(2\sigma_2)sin(\phi)))\right] \quad (70b)$$

$$Y_{eff,C} = \frac{csc^2(\sigma_1)sec^2(\sigma_2)}{Z_1}\left[2sin(\phi)(-2\gamma cos(\theta)sin(\theta-\phi) + \beta cos(\phi)sin(\sigma_2)cos(\sigma_2))\right. \\ \left. + j(cos(\sigma_1)cos^2(\sigma_2)sin(\sigma_1) + sin(\phi)(-4\gamma cos(\theta)cos(\theta-\phi) + \beta sin(2\sigma_2)sin(\phi)))\right] \quad (70c)$$

$$Y_{eff,D} = \frac{csc^2(\sigma_1)sec^2(\sigma_2)}{Z_1}\left[sin(\phi)(-\beta cos(\phi)sin(2\sigma_2) + 4\gamma cos(\theta)sin(\theta+\phi))\right. \\ \left. - j(cos(\sigma_1)cos^2(\sigma_2)sin(\sigma_1) + sin^2(\phi)(2\gamma sin(2\theta) - \beta sin(2\sigma_2)) - 2\gamma cos^2(\theta)sin(2\phi))\right] \quad (70d)$$

## 5.3. Output Power Control

As with the lumped combiner implementation, in the case of the TL combiner, output power control can be achieved by adjusting the signal amplitudes at the combiner inputs $V_S$ (by modulating the PA drive amplitudes and/or their supply voltages), or by adjusting their outphasing angles $\theta$ and $\phi$ (see Fig. 5-3). Straightforward transmission-line analysis reveals that the load current $I_L$ of the TL combiner of Fig. 5-1 depends on the terminal voltage phasors $V_A$-$V_D$ and is given by (71):

$$I_L = j\frac{sec(\sigma_2)}{Z_1 sin(\sigma_1)}(V_A + V_C - V_B - V_D). \quad (71)$$

Assuming the phasor relationship between the combiner port voltages is as given by (17), then $I_L$ can be expressed in terms of the outphasing angles $\theta$ and $\phi$, and the PA drive amplitude $V_S$:

$$I_L = \frac{4V_S sin(\phi)cos(\theta)}{Z_1 cos(\sigma_2)sin(\sigma_1)}. \quad (72)$$

From here, one can easily compute the output power $P_{out}$ that the combiner delivers to the load $R_L$. Note that by selecting $Z_1 = X_1/\sin(\sigma_1)$ and $Z_2 = X_2/\sin(\sigma_2)$, where $X_1$ and $X_2$ are the branch reactances of the lumped combiner of Fig. 2-5, in the limit of $\sigma_1$ and $\sigma_2$ being zero (73) also reduces to the equation for output power (35) in the case of the lumped combiner implementation.

$$P_{out} = \frac{8R_L V_S^2}{Z_1^2 sin^2(\sigma_1)cos^2(\sigma_2)}sin^2(\phi)cos^2(\theta). \quad (73)$$

Similar to the lumped combiner implementation, for $\theta = 0$ and $\phi = 90°$, the output power saturates to its saturation level $P_{out,sat}$ given by (74).

$$P_{out,sat} = \frac{8R_L V_S^2}{Z_1^2 \sin^2(\sigma_1)\cos^2(\sigma_2)}. \tag{74}$$

## 5.4. Outphasing Control Strategies

It can be seen from (73) that, just as in the case of the lumped combiner implementation, the output power $P_{out}$ depends on both $\theta$ and $\phi$. Although infinitely many possible control angle pairs exist for a given desired output power level, only a particular pair may be selected due to additional requirements on the behavior of the combiner. This section explores adapting the optimal-phase (OP) and optimal-susceptance (OS) control methodologies introduced earlier to the case of the transmission-line combiner implementation.

### 5.4.1. Optimal-Susceptance Control

As was already described in Section 2.5.2, optimal-susceptance control entails the selection of the control angle pair $[\theta, \phi]$ so that the combiner will deliver the desired output power level while minimizing the peak susceptive loading of the PAs over the entire output power operating range. The OS control angles can be calculated by employing the output power relation (73), and further imposing identical susceptive components (by magnitude) of the TL combiner effective input admittances (70), i.e. $|\mathrm{Im}(Y_{eff,A})| = |\mathrm{Im}(Y_{eff,B})| = |\mathrm{Im}(Y_{eff,C})| = |\mathrm{Im}(Y_{eff,D})|$. Equations (75) and (76) give the OS control angles in terms of the desired output power $P_{out}$.

$$\phi = \tan^{-1}\left(\frac{Z_1 \tan(\sigma_1) P_{out}}{2V_S^2}\right) \tag{75}$$

$$\theta = \cos^{-1}\left(\cos(\sigma_2)\cos(\sigma_1)\sqrt{\frac{4V_S^4 + P_{out}^2 Z_1^2 \tan^2(\sigma_1)}{8R_L V_S^2 P_{out}}}\right) \tag{76}$$

Fig. 5-4 illustrates the input admittance characteristics of an example design of the TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 567\ \Omega$, $\sigma_1 = 0.0628$, $\sigma_2 = 0.0861$, and $R_L = 50\ \Omega$ as a result of the OS outphasing control. Referring to Fig. 5-1 and Fig. 2-7, it is easy to see that the admittance characteristics of the TL and lumped combiner implementations are approximately equivalent. The input conductance is modulated in accordance with output power, while peak susceptance variations are limited to less than 2.5 mS. Note that in the example design considered here fairly large transmission-line characteristic impedances of 567 Ω are used. Although the implementation of such transmission lines in reality may pose some challenges, the

purpose of this example is to demonstrate that a TL combiner can be designed to have almost identical characteristics as its lumped-element counterpart. As will be discussed shortly, the higher the transmission-line characteristic impedance relative to the load impedance, the closer the TL combiner mimics the behavior of the lumped-element combiner. On the other hand, smaller transmission-line impedances will result in slightly wider operating range at the expense of higher susceptance (and phase) variations in the input admittances of the combiner. For example, Fig. 5-5 depicts the effective input admittance characteristics of each of the combiner input ports A-D of an example design of the TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 100\ \Omega$, $\sigma_1 = 0.3640$, $\sigma_2 = 0.5096$, and $R_L = 50\ \Omega$ as a result of OS outphasing control. Comparing the susceptance characteristics of Fig. 5-4 and Fig. 5-5 reveals that decreasing the transmission-line characteristic impedances for a given combiner load $R_L$ does indeed result in larger phase and susceptance variations (and slightly wider operating range). In the former combiner example ($Z_1 = Z_2 = 567\ \Omega \approx 11R_L$) the peak admittance phase and susceptance are 2° and 2.5 mS respectively, while in the later example ($Z_1 = Z_2 = 100\ \Omega = 2R_L$) the peak admittance phase and susceptance have dramatically increased to approximately 15° and 20 mS respectively.

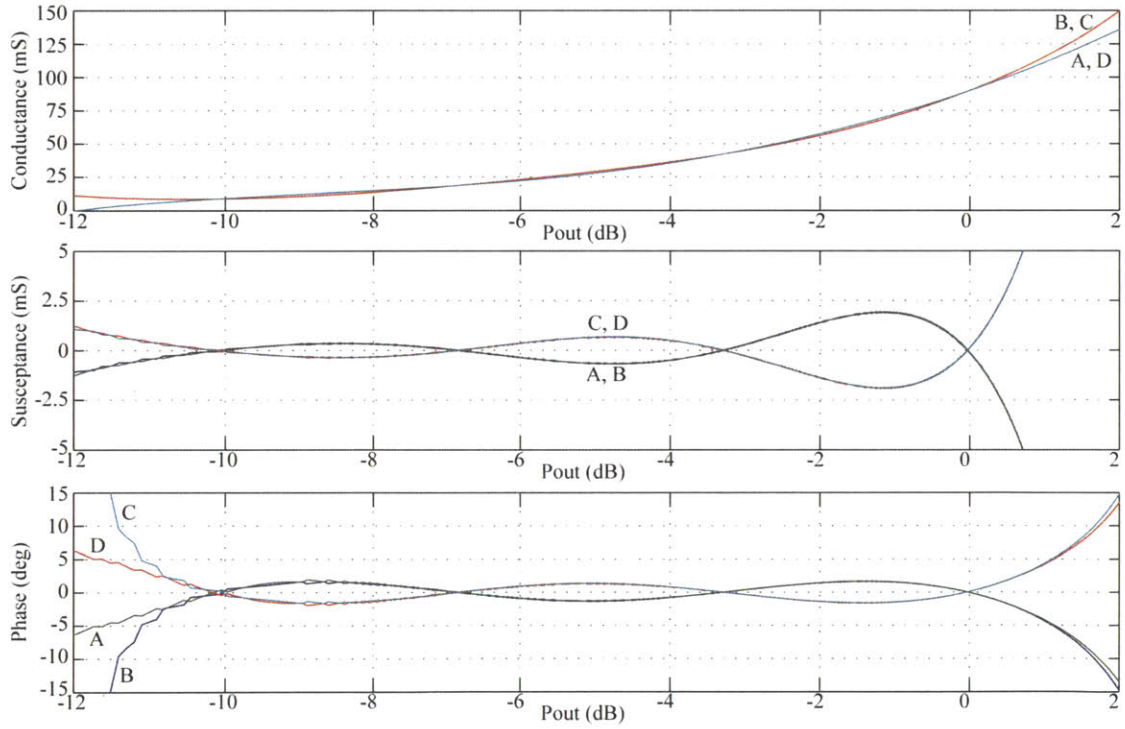



Fig. 5-4: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 567\ \Omega$, $\sigma_1 = 0.0628$, $\sigma_2 = 0.0861$, and $R_L = 50\ \Omega$ as a result of the OS outphasing control.

The above example comparison suggests that in order for the TL combiner implementation to exhibit approximately the same behavior as its lumped-element counterpart, the characteristic impedance of the transmission lines in Fig. 5-1 must be selected to be significantly larger than the combiner loading

impedance $R_L$ (by a factor of ten or larger). In a typical RF application where the intended load is 50 Ω, similarly to the above example, one must use transmission lines with characteristic impedance on the order of 500 Ω or higher. The implementation of transmission lines with such high characteristic impedances may be quiet problematic however. This is where one can appreciate the design flexibility introduced by an impedance transformation stage at the combiner's output. Suppose for example that one desires to drive a 50 Ω load with the TL combiner of Fig. 5-1. However, instead of designing the combiner network for a 50 Ω load, it can be designed for 12.5 Ω. An additional impedance transformation stage (with a transformation factor of 4) can be employed at the combiner's output to transform the actual 50 Ω load to a 12.5 Ω combiner loading impedance $R_L$. As a consequence, the characteristic impedance of the combiner's transmission lines can be selected on the order of 125 Ω – a value that is significantly easier to implement than 500 Ω in the case of the combiner driving the 50 Ω load directly. Of course, in the latter case one must also redesign the PAs to handle the new loading impedance requirements: the combiner designed for a 12.5 Ω load will have effective input admittances that are a quarter of those of the combiner designed to operate with a 50 Ω load. The MATLAB script employed in simulating the TL combiner and generating Fig. 5-4 and Fig. 5-5 can be found in Appendix C (combiner4_outphasing_control_TL.m).

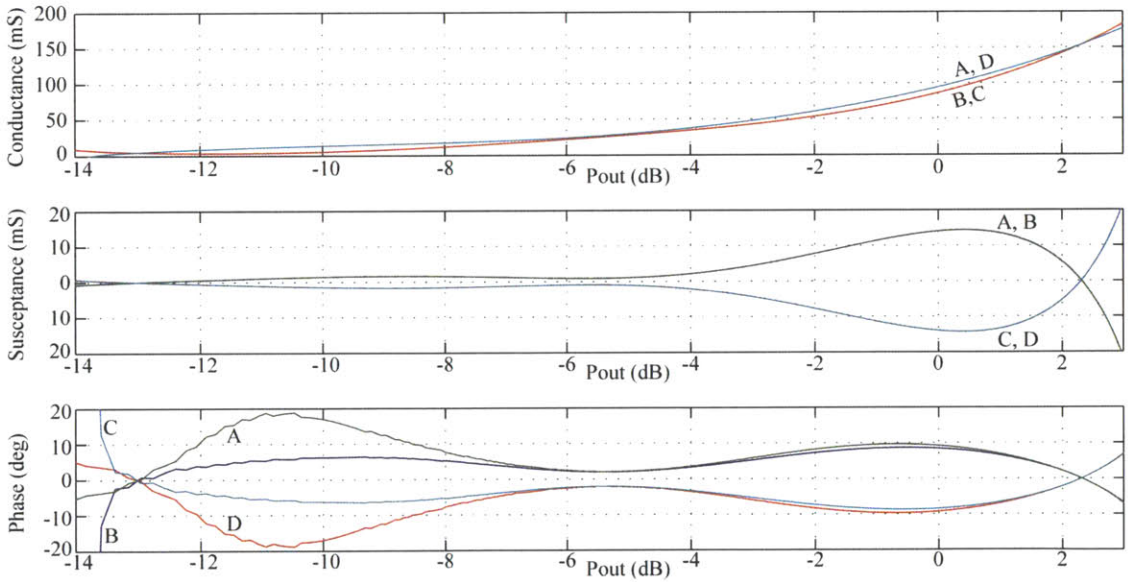



Fig. 5-5: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 100\ \Omega$, $\sigma_1 = 0.3640$, $\sigma_2 = 0.5096$, and $R_L = 50\ \Omega$ as a result of the OS outphasing control.

### 5.4.2. Optimal-Phase Control

By analogy to OS control, optimal-susceptance control entails the selection of the control angle pair [θ, ϕ] so that the combiner will deliver the desired output power level while minimizing the peak phase of the TL combiner's input admittances seen by the PAs over the entire output power operating range. Although close-form expressions for the OP control angles have not been determined, they can be easily computed numerically for any arbitrary combiner design. A MATLAB script that numerically determines these angles for any four-way TL combiner design is included in Appendix C (combiner4_outphasing_control_TL.m). Fig. 5-6 illustrates the input admittance characteristics of an example design of the TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 567\ \Omega$, $\sigma_1 = 0.0628$ and $\sigma_2 = 0.0861$ (the same TL combiner design as in the example above) as a result of the OP outphasing control. Not surprisingly, as can be seen from Fig. 5-4 and Fig. 5-6, both the OP and OS control methods result in approximately identical input admittance characteristics. In fact, Fig. 5-7 shows that the OP and OS control angles, for all practical purposes, are identical over almost the entire combiner operating range. Similarly to the lumped-element combiner implementation, by outphasing the TL combiner for minimum susceptive variations, one simultaneously achieves minimum input admittance phase variations, and vice-versa.

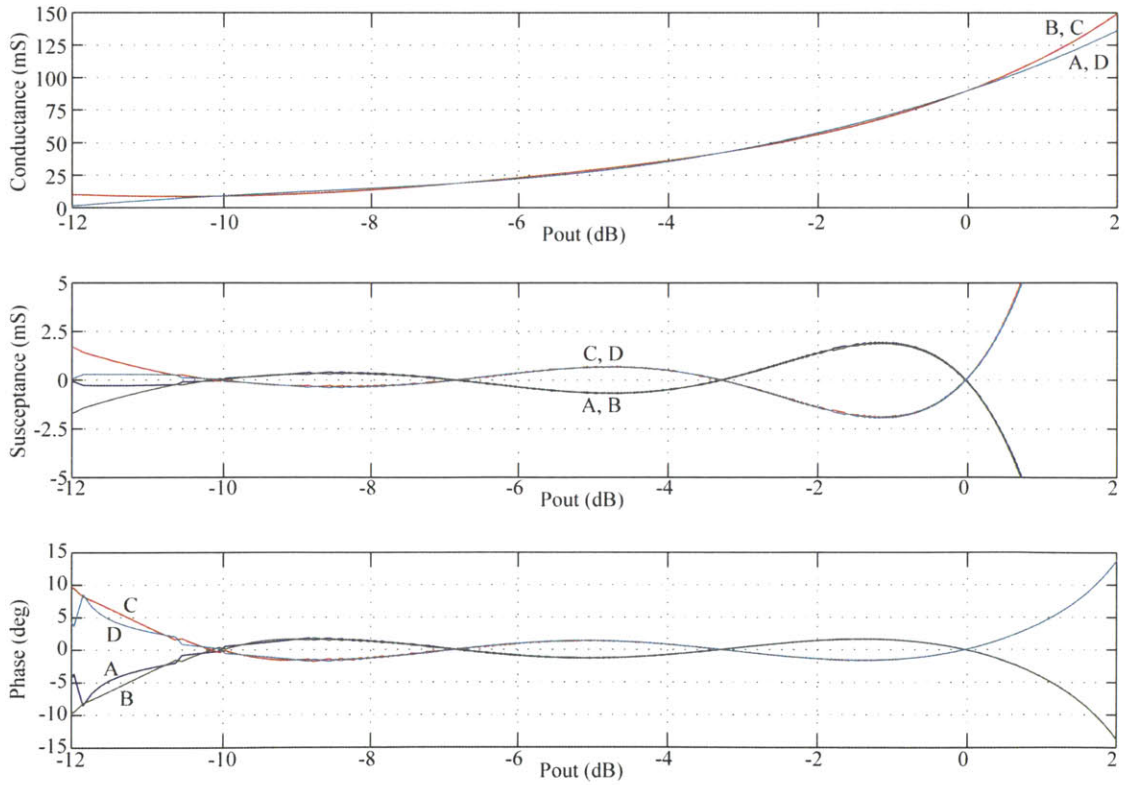



Fig. 5-6: Effective input conductance (top), susceptance (middle), and phase (bottom) seen by each of the PAs (A-D) driving the four-way TL combiner of Fig. 5-1 with $Z_1 = Z_2 = 567\ \Omega$, $\sigma_1 = 0.0628$, $\sigma_2 = 0.0861$, and $R_L = 50\ \Omega$ as a result of the OP outphasing control.

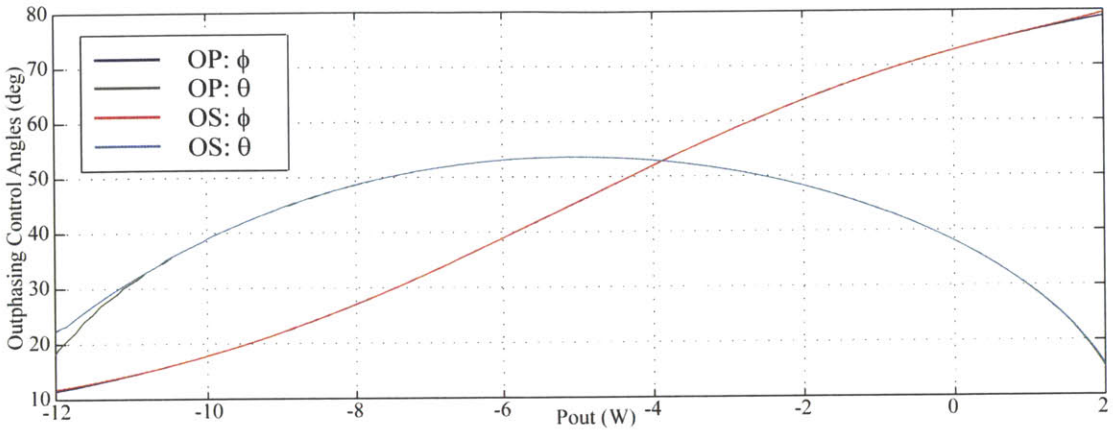



Fig. 5-7: Outphasing control angles θ and ϕ for the Optimal Phase (OP) and Optimal Susceptance (OS) control methods for the four-way combiner of Fig. 5-1 with $Z_1 = Z_2 = 567\ \Omega$, $\sigma_1 = 0.0628$, $\sigma_2 = 0.0861$, and $R_L = 50\ \Omega$.

## 5.5. Design Methodologies

The methodology presented here for designing the transmission-line combiner of Fig. 5-1 is very similar to the one employed for designing the lumped-element combiner (see Section 2.6). The design of the TL combiner begins with a specification on its operating output power range and its load $R_L$. As will be discussed shortly, a design parameter k is selected based on the intended combiner operating range. The reactance values $X_1$ and $X_2$ are then calculated according to (77) and (78). Note that these reactances are equivalent to the branch reactances of the lumped-element combiner in Fig. 2-5; this is the starting point for converting the lumped-element implementation into the transmission-line implementation.

$$X_2 = \frac{2R_L}{k+1} \tag{77}$$

$$X_1 = \frac{X_2}{k + \sqrt{k^2 - 1}} \tag{78}$$

For given transmission-line characteristic impedances $Z_1$ and $Z_2$, the transmission-line length increments $\Delta L_1$ and $\Delta L_2$ can then be computed according to (79) and (80). The higher the values of $Z_1$ and $Z_2$, are selected, the closer is the behavior of the TL combiner to that of its lumped-element counterpart.

$$\Delta L_1 = \frac{1}{2\pi} sin^{-1}\left(\frac{X_1}{Z_1}\right) \tag{79}$$

$$\Delta L_2 = \frac{1}{2\pi} sin^{-1}\left(\frac{X_2}{Z_2}\right) \tag{80}$$

A set of design curves analogical to the ones presented in Fig. 2-13 are shown in Fig. 5-8 for the TL combiner for various transmission-line characteristic impedances ranging from $2R_L$ to $10R_L$ Ω. To determine the appropriate design factor for a particular TL combiner operating output power range ratio (PRR), start from the left Zero-Point Power Ratio axis and trace the desired PRR to a black curve corresponding to the selected transmission-line characteristic impedances $Z_1$ and $Z_2$. Tracing then vertically down to the k-value axis yields the appropriate value of k. The resultant peak susceptive PA loading (normalized to $1/R_L$) for the chosen value of k is then given by tracing the k value vertically up to a red curve corresponding to the values of $Z_1$ and $Z_2$, and then tracing horizontally (right) to the Susceptance axis. It is interesting to note that although higher $Z_1$ and $Z_2$ values result in a TL combiner whose behavior closely mimics that of the lumped-element combiner, smaller $Z_1$ and $Z_2$ values yield wider output power operating range at the expense of larger peak susceptance variations. The design curves in Fig. 5-8 are generated for transmission lines having identical characteristic impedances, which may result in certain simplifications to the constriction of the combiner. However, similar design curves can be generated for any arbitrary combination of $Z_1$ and $Z_2$ values. A MATLAB script for generating such design curves is included in Appendix C (combiner4_design_curves.m).

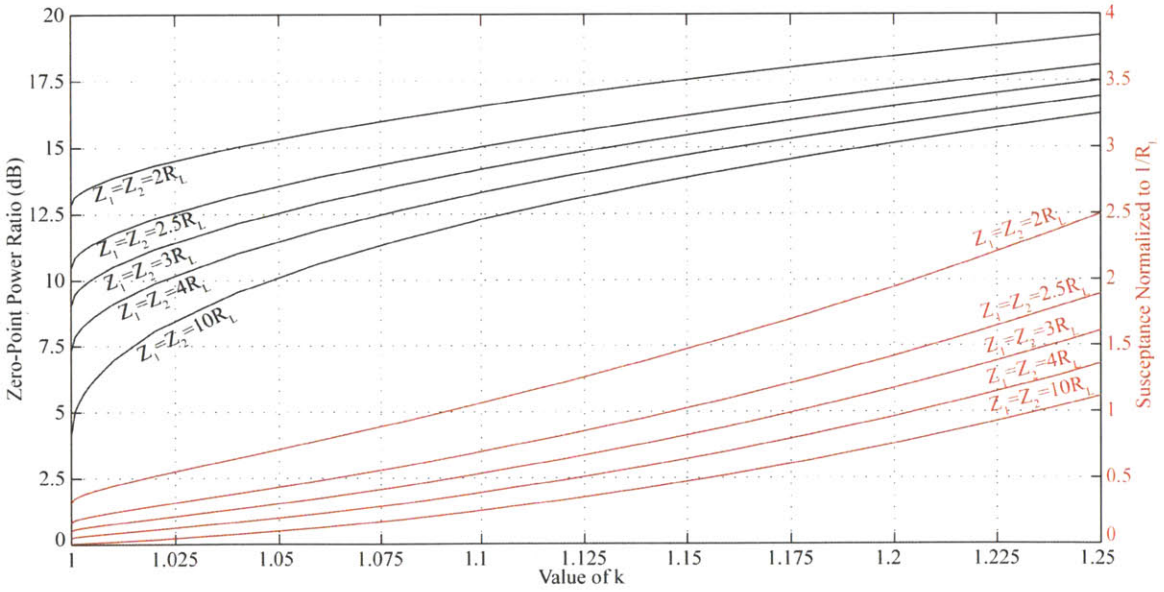



Fig. 5-8: Four-way TL combiner design curves: trace-out the specified power range ratio to the Power Ratio Curve to determine the appropriate design value for k for particular transmission line characteristic impedances. The Susceptance Curves give the corresponding peak effective input susceptance that a PA can see at the inputs ports of the combiner over the specified operating range for OP/OS outphasing control. The susceptance axis is normalized to a combiner load $R_L = 1$ Ω; to denormalize, multiply axis by $1/R_L$.

# Chapter 6

# Conclusion

Many of today's modern RF power amplification systems are required to provide dynamic control of their output power over a wide operating power range. Conventionally, to achieve their performance specifications, such systems typically employ linear power amplifiers whose output power can be easily controlled over a wide operating range through direct amplitude modulation of their drive signals. Unfortunately, the efficiency of linear power amplifiers degrades rapidly with output power back-off, and consequently results in poor overall system efficiency. On the other hand, nonlinear, switch-mode power amplifiers are characterized with higher operating efficiencies, although dynamic control of their output power over a wide power range is a challenging task especially for the bandwidth requirements of modern RF systems. Nevertheless, the ability to replace linear amplifiers in conventional RF power amplification systems with more efficient non-linear amplifiers is highly desired, and it is an important step toward improving the overall system efficiency.

## 6.1. Summary

This thesis describes the development of a new multi-way power combing and outphasing system that provides ideally lossless power combining from four or more PAs, along with nearly-resistive loading of the individual power amplifiers over a very wide output power range. The proposed combiner architecture can be used with both linear and nonlinear PAs. Control of the combiner's output power is achieved either through outphasing of the individual PAs, or through modulation the amplitude of the inputs to the combiner (such as by drain modulation of the PAs or direct amplitude modulation of the PA drive signals).

Chapter 2 discusses the fundamentals of operation of the proposed power combiner. It addresses the synthesis of this new combiner architecture and explores in detail its input/output-port characteristics. The variation of the combiner's input-port admittances with modulation of its output power is thoroughly examined, and various PA outphasing methodologies are presented for controlling the combiner's output power. A useful combiner design methodology is outlined, and numerous implementation topologies are discussed.

The implementation of an actual outphasing and power combining system prototype operating at 27.12 MHz and combining power from four class-E switched-mode amplifiers is described in Chapter 3. Each of the Class-E PAs is designed to provide a peak output power of 25 W, while the combiner's output power can be controlled over a 10 dB power range (from 10 W to 100 W) by appropriate outphasing of the PAs. The design and implementation of the various sub-system components such as the PAs, the combiner, the outphasers and the digital controller are addressed in detail.

Chapter 4 evaluates experimentally the performance of the implemented outphasing and combining system. It demonstrates that the proposed PA outphasing methods are effective in controlling the combiner's output power while preserving a resistive loading of the PAs over the entire 10 dB operating range. Furthermore, power efficiency measurements of the implemented system reveal dramatic efficiency improvements over a linear PA-based amplification system.

Chapter 5 presents a transmission-line (TL) implementation of the proposed combiner suitable for power combining applications at very high frequencies (such as UHF and above) where transmission lines have advantages over discrete components. The key performance characteristics of the TL combiner such as its input-port admittance behavior, and various outphasing methodologies for controlling its output power are discussed. A TL combiner design procedure is included which facilitates the selection of the various parameters of the transmission-lines making-up the combiner.

The work presented in this thesis lays-down the foundation of the proposed lossless multi-way power combining architecture, and it can be used as a guide in the future design of various multi-way power combining systems.

## 6.2. Directions for Future Work

The purpose of the work presented in this thesis is to develop and discuss the fundamentals of a new power combining and outphasing architecture, and to experimentally verify its key performance characteristics. However, several aspects of the proposed power combining system have been left as a subject for future explorations.

Although in the present design, the outphasing control angles of the PAs were continuously monitored and manually adjusted in real-time to reflect the required phase shift between the PAs, this is not a luxury that one can afford in a real-life system implementation. An additional feedback system (such as a Phased-Locked Loop) may have to be implemented to monitor the outphasing angles of the PAs and adjust them automatically to their appropriate values.

In addition, this thesis has only explored the static behavior of the combiner, i.e. the behavior of the combiner once it has reached its steady-state. It would be valuable to examine the transient effect of the combiner. However, as the system's transient behavior is highly dependent on the type of power amplifiers used to drive the combiner and the specific application requirements the system is designed for, it has been left as the subject of a future study.

Moreover, this thesis has predominantly focused on the implementation of a four-way combiner. Although the concepts have been extended for the case of a general multi-way combiner, it would be of merit to evaluate the performance of an actual power amplification system that combines power from more than four PAs and compare it to that of the four-way combiner presented here.

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## Appendix A

# Design of Multi-Stage RCNs

The structure, design and behavior of a single-stage RCN were already discussed in Section 2.1. Multi-stage RCNs offer the possibility of even smaller input resistance variations (or wider load resistance ranges) than single-stage designs. This appendix presents a general recursive procedure for designing a multi-stage RCN to provide an input resistance that deviates by a specified peak amount away from a desired median input resistance value, and determining the load resistance range over which this can be accomplished.

## A.1. Design Methodology

Consider the generalized N-stage RCN shown in Fig. A-1. Each of the $2^N$ $R_o$ resistances simultaneously varies over a particular operating range $[X_1/b_1, b_1X_1]$ and serves as the load resistance of the $2^{N-1}$ single-stage RCNs comprising the first stage. Respectively, each of the input resistances $R_{in,1}$ varies over the compressed range $[X_1, k_1X_1]$ and in turn serves as the load resistance of the second stage RCN stage, etc. The relationship between the corresponding k and b values for any particular single stage is given by (A1).

$$b = k + \sqrt{k^2 - 1} \text{ and } k = \frac{1+b^2}{2b} \tag{A1}$$

Suppose that it is desired to design the RCN of Fig. A-1 to provide an input resistance $R_{in,N}$ within $\pm\Delta R_N$ of a desired median value $R_{in,N,med}$ over as wide range of $R_o$ as possible. To accomplish this, first select a $k_N$ value (stage N input resistance ratio) of

$$k_N = \frac{R_{in,N,med} + \Delta R}{R_{in,N,med} - \Delta R} \tag{A2}$$

and compute the corresponding stage N reactance magnitude.

$$X_N = \frac{2R_{in,N,med}}{k_N + 1} = \frac{2\Delta R_N}{k_N - 1}, \tag{A3}$$

Consequently, the $b_N$ value (stage N load resistance ratio), is given by:

$$b_N = k_N + \sqrt{k_N^2 - 1}\,. \tag{A4}$$

To determine the optimal value of the N-1 stage reactance, we must consider that in order to satisfy the original range specification on $R_{in,N}$, $R_{in,N-1}$ must be constrained to $[X_N/b_N, X_N b_N]$. Thus, similarly to $R_{in,N}$, we demand that variations of $R_{in,N-1}$ are limited to within $\Delta R_{N-1}$ of some median value $R_{in,N-1,med}$, where

$$R_{in,N-1,med} = \frac{X_N b_N + X_N / b_N}{2} \quad \text{and} \quad \Delta R_{N-1} = \frac{X_N b_N - X_N / b_N}{2}\,. \tag{A5}$$

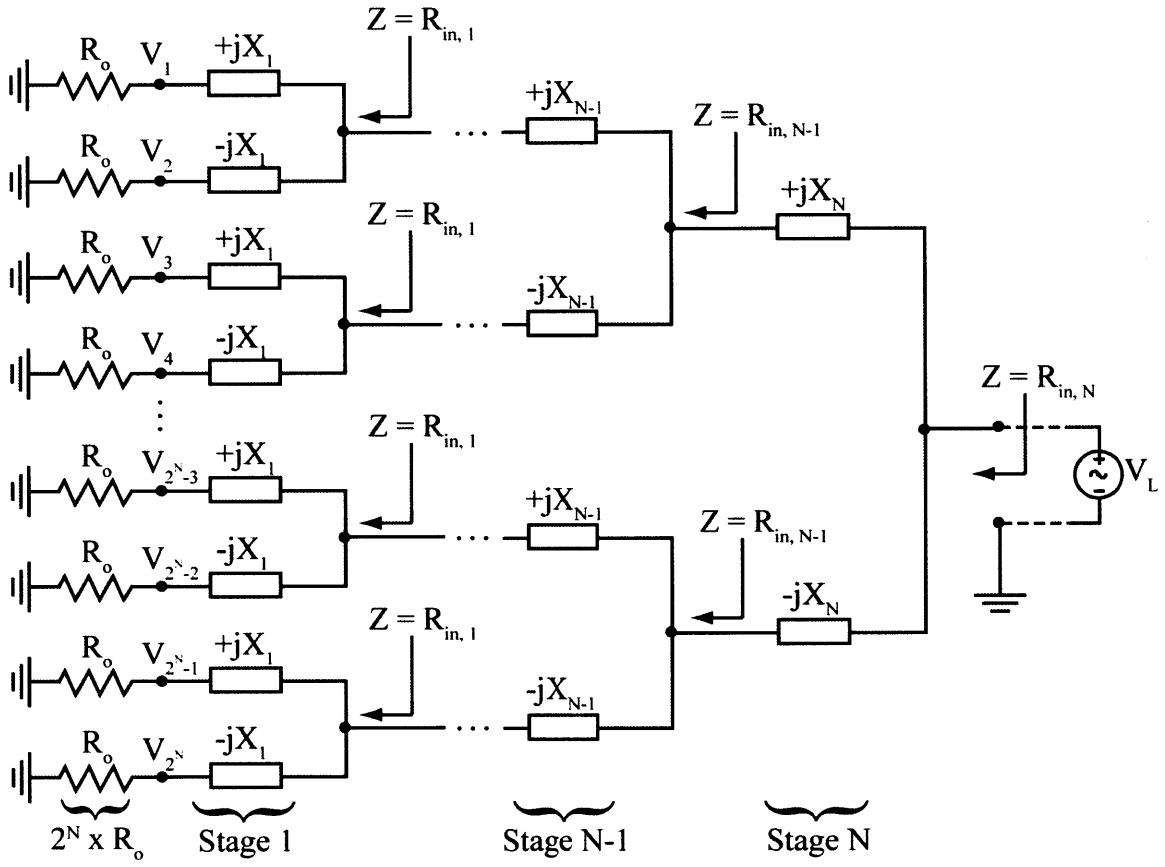



Fig. A-1: N-stage resistance compression network obtained by cascading number of single-stage RCN networks. The input resistance $R_{in,N}$ seen by the voltage source $V_L$ varies over a much smaller range compared to that of the $2^N$ matched load resistances $R_o$.

Given (A5) and employing (A2) and (A3), values for $k_{N-1}$, $b_{N-1}$ and $X_{N-1}$ are straightforward to compute and in turn can be utilized for formulating the next set of corresponding constraints on $R_{in,N-2,med}$ etc. It can be shown that this iterative procedure can be simplified to a set of two recursive equations (A6) which allow the computation of $X_{n-1}$ and $b_{n-1}$ for any n, $2 \le n \le N$ provided that $X_n$ and $b_n$ are known.

$$X_{n-1} = \frac{X_n}{b_n} \quad \text{and} \quad b_{n-1} = b_n^2 + \sqrt{b_n^4 - 1} \tag{A6}$$

This process is repeated until reactance magnitudes for all stages have been determined. Fig. A-2 depicts how the input resistance $R_{in,N}$ varies as a function of load resistance $R_o$ for the general N-stage RCN of Fig. A-1 when compression network reactance values are selected as described above. It can be shown that for any N-stage RCN, $R_{in,N}$ will exhibit exactly $2^{N-1}$-1 local maxima ($R_{in,N} = k_N X_N$) and $2^{N-1}$ local minima ($R_{in,N} = X_N$) within its operating range $R_o \in [X_1 / b_1, X_1 b_1]$. In addition, for $R_o \leq X_1/b_1$ and $R_o \geq X_1 b_1$, $R_{in,N}$ is always increasing monotonically. Moreover, it can be demonstrated that the equation $R_{in,N} = R_{in,N,med}$ has exactly $2^N$ real roots (illustrated with the emphasized intersection points in Fig. A-2). The importance of this subtle fact will become apparent later when we consider the design and performance of multi-stage power combiner networks.

Suppose that the RCN of Fig. A-1 is now driven with a voltage source $V_L$. It is useful to consider the general sinusoidal steady-state relationship between the voltages $V_1 - V_{2^N}$ across the $2^N$ load resistors $R_o$ and the voltage $V_L$. It can be shown that for a given selection of values of the RCN's reactive components, this relationship is expressed by (A7), where f and $g_n$ are scalar functions dependant only on the RCN component values and the load resistances $R_o$. In addition, any phase shift in the driving signal $V_L$ will outphase all load voltages by the same amount. Furthermore, it can be demonstrated that phases $\varphi_1 - \varphi_{2^N}$ are distributed symmetrically, i.e. $\varphi_1 = -\varphi_{2^N}$, $\varphi_2 = -\varphi_{2^N-1}$, etc.

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{2^N} \end{bmatrix} = V_L f\left(R_o, X_1, \cdots, X_{2^N}\right) \begin{bmatrix} e^{j\varphi_1} \\ e^{j\varphi_2} \\ \vdots \\ e^{j\varphi_{2^N}} \end{bmatrix} \tag{A7}$$

$$\varphi_n = g_n\left(R_o, X_1, \cdots, X_{2^N}\right) \text{ for } 1 \leq n \leq 2^N$$

Three special cases of the general N-stage RCN (single-stage, two-stage, and three-stage designs) are discussed below which will prove particularly useful for understanding the behavior of multi-stage power combiners and their corresponding outphasing control laws.

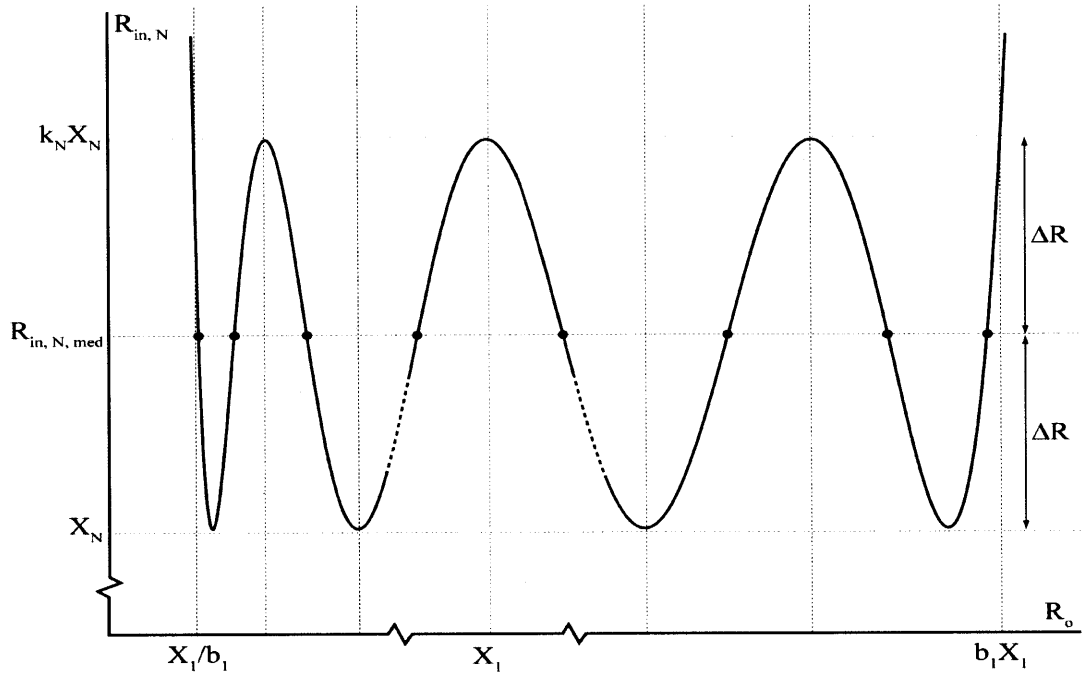



Fig. A-2: Resistive input impedance $R_{in,\,N}$ as a function of the matched load resistance value $R_o$ for the N-stage compression network of Fig. A-1. Selection of the compression network reactances as described provides this characteristic, which compresses resistance to a greater extent than is possible in a single-stage RCN design.

## A.2. Single-Stage Resistance Compression Network

Fig. A-3 shows a single-stage resistance compression network driven by a voltage source $V_L$. For the sake of completeness, this sub-section summarizes key results along with important relationships for the single-stage RCN. The input impedance (entirely resistive) as seen by the source $V_L$ is given by (A8).

$$R_{in,1} = \frac{R_o^2 + X_1^2}{2R_o} \tag{A8}$$

The phasor representation of the voltages across each matched load resistor $R_o$ is:

$$\begin{bmatrix} V_A \\ V_B \end{bmatrix} = V_L \frac{R_o}{\sqrt{R_o^2 + X_1^2}} \begin{bmatrix} e^{-j\phi} \\ e^{+j\phi} \end{bmatrix} \tag{A9}$$

$$\phi = \mathrm{ATAN}\left(\frac{X_1}{R_o}\right). \tag{A10}$$

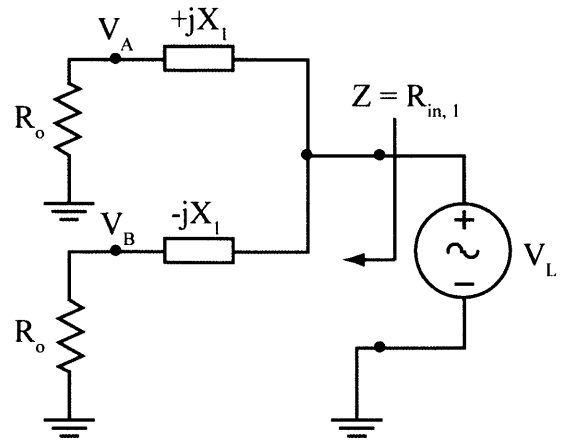



Fig. A-3: Single-stage resistance compression network, driven by a voltage source $V_L$.

## A.3. Two-Stage Resistance Compression Network

A two-stage RCN driven by a voltage source $V_L$ is depicted in Fig. A-4. The input resistance as seen by the driving source is given by (A11). Equations (A12)-(A14) express the dependence of load voltages $V_A$-$V_D$ in terms of the drive voltage $V_L$.

$$R_{in,2} = \frac{\left(\frac{R_o^2 + X_1^2}{2R_o}\right)^2 + X_2^2}{\frac{R_o^2 + X_1^2}{R_o}} \tag{A11}$$

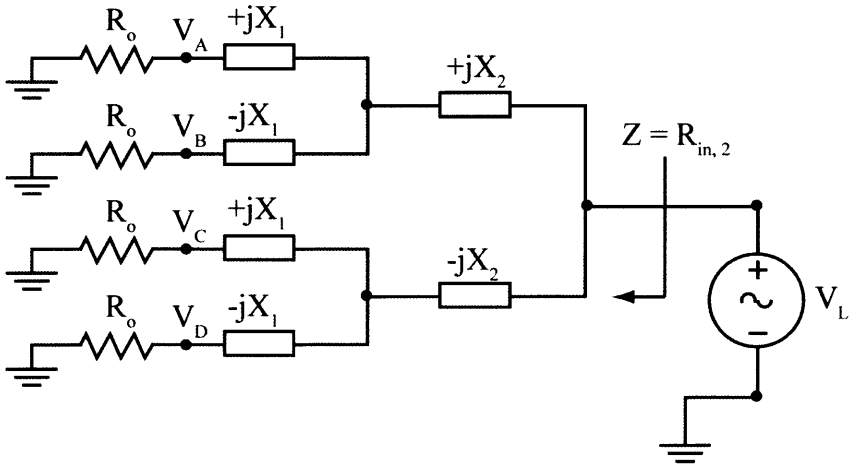



Fig. A-4: Two-stage resistance compression network, driven by a voltage source $V_L$.

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_L \frac{\sqrt{R_o^2 + X_1^2}}{2\sqrt{\left(\frac{R_o^2 + X_1^2}{2R_o}\right)^2 + X_2^2}} \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{+j\phi}e^{-j\theta} \\ e^{-j\phi}e^{+j\theta} \\ e^{+j\phi}e^{+j\theta} \end{bmatrix} \tag{A12}$$

$$\theta = \text{ATAN}\left(\frac{2R_oX_2}{R_o^2 + X_1^2}\right) \tag{A13}$$

$$\phi = \text{ATAN}\left(\frac{X_1}{R_o}\right). \tag{A14}$$

## A.4. Three-Stage Resistance Compression Network

Schematic of a three-stage RCN is shown in Fig. A-5. The input resistance seen by the source $V_L$ is given by (A15). The phasor load voltages $V_A$-$V_H$ are related to the driving voltage $V_L$ via (A16) with the phase angles respectively given by (A17-A19).

$$R_{in,3} = \frac{R_{in,2}^2 + X_3^2}{2R_{in,2}}, \text{ where } R_{in,2} = \frac{\left(\frac{R_o^2 + X_1^2}{2R_o}\right)^2 + X_2^2}{\frac{R_o^2 + X_1^2}{R_o}} \tag{A15}$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \\ V_E \\ V_F \\ V_G \\ V_H \end{bmatrix} = V_L \frac{\sqrt{\left(X_1^2 + R_o^2\right)^2 + 4X_2^2R_o^2}}{4\sqrt{R_o^2 + X_1^2}\sqrt{\left(\frac{4R_o^2X_2^2 + \left(X_1^2 + R_o^2\right)^2}{4R_o\left(X_1^2 + R_o^2\right)}\right)^2 + X_3^2}} \begin{bmatrix} e^{-j\phi}e^{-j\theta}e^{-j\psi} \\ e^{+j\phi}e^{-j\theta}e^{-j\psi} \\ e^{-j\phi}e^{+j\theta}e^{-j\psi} \\ e^{+j\phi}e^{+j\theta}e^{-j\psi} \\ e^{-j\phi}e^{-j\theta}e^{+j\psi} \\ e^{+j\phi}e^{-j\theta}e^{+j\psi} \\ e^{-j\phi}e^{+j\theta}e^{+j\psi} \\ e^{+j\phi}e^{+j\theta}e^{+j\psi} \end{bmatrix} \tag{A16}$$

$$\psi = \text{ATAN}\left(\frac{4R_oX_3\left(X_1^2 + R_o^2\right)}{4R_o^2X_2^2 + \left(X_1^2 + R_o^2\right)^2}\right) \tag{A17}$$

$$\theta = \text{ATAN}\left(\frac{2R_oX_2}{R_o^2 + X_1^2}\right) \tag{A18}$$

$$\phi = \text{ATAN}\left(\frac{X_1}{R_o}\right) \tag{A19}$$

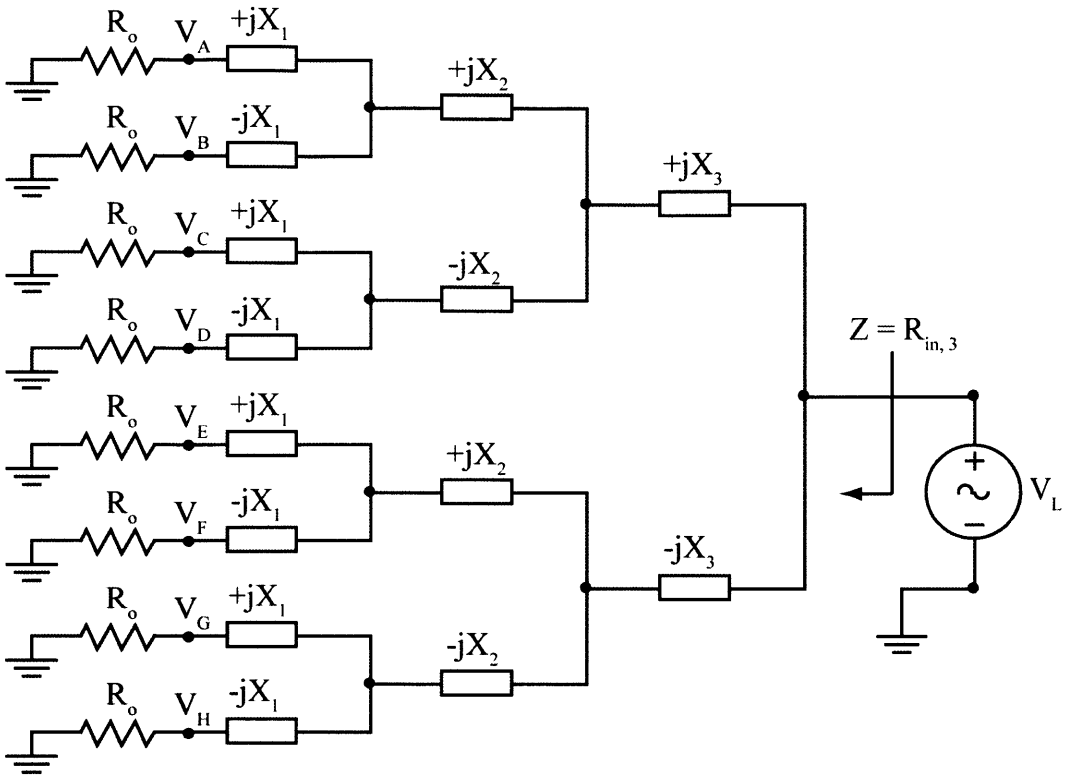



Fig. A-5: A three-stage resistance compression network, driven by a voltage source $V_L$

## Appendix B

# Multi-Way Power Combining

Chapter 2 has already laid-out the four-way combiner fundamentals, and it has thoroughly addressed its design, implementation and key performance characteristics. This appendix aims to expand and generalize the already presented power combining concepts to the case of the N-way combiner. Furthermore, it briefly explores the design and performance of the eight-way combiner as a special case of the generalized N-way combiner.

## B.1. Synthesis of the N-Way Power Combiner

Consider the N-stage RCN shown on Fig. A-1 driven by a voltage source $V_L$. Suppose that the sign of every reactive and resistive component in this network is negated. This is equivalent to taking the network of Fig. A-1 and applying type-I time-reversal duality followed by type-III time-reversal duality [54], [55]. Neglecting the impact upon the natural response of the circuit, the sinusoidal steady-state behavior of such a circuit would have all current flow directions reversed, while preserving voltage relationships, thus yielding reversed power flow (i.e. from the – now negative – resistors to the voltage source $V_L$). The ratio of the voltage $V_L$ to the current flowing into the source would be that of $R_{in,N}$ of the original compression network, which is close to the value of $R_{in,N,med}$. Likewise, the voltages across the now-negative resistors would be respectively equivalent to the ones in the original network (A7), and currents proportional to these voltages would flow into the network (i.e. the apparent impedances seen looking into the network ports to which the negative resistances are connected would be resistive with values $|R_o|$) [29].

To develop a power combining and outphasing system, one can take advantage of the above observations. In particular, replace the source $V_L$ in Fig. A-1 with a load resistance $R_L = R_{in,N,med}$ and replace the resistors $R_o$ with voltage sources (or power amplifiers in practice). This leads directly to the system of Fig. B-1. By controlling the phases of the sources (B1) to match their behavior in the original N-stage resistance compression network, one can obtain power control over a wide range while preserving nearly resistive loading of the sources. While these substitutions do not lead to precise duality between RCNs and the proposed power combining and outphasing system, they provide the means to develop effective outphasing and power combing systems [29].

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{2^N} \end{bmatrix} = V_S \begin{bmatrix} e^{j\varphi_1} \\ e^{j\varphi_2} \\ \vdots \\ e^{j\varphi_{2^N}} \end{bmatrix} \tag{B1}$$

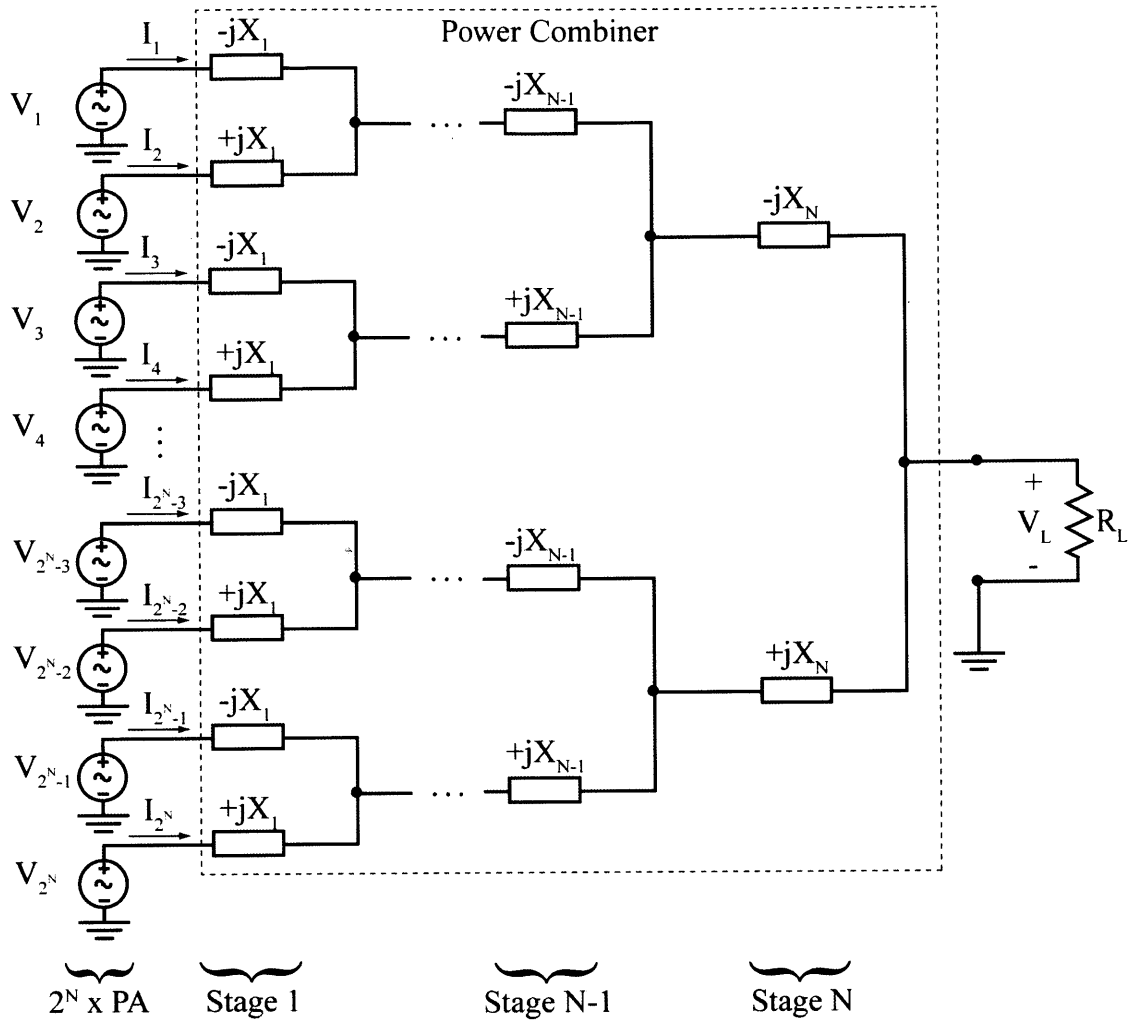



Fig. B-1: A General N-stage example implementation of the proposed power combiner system. This implementation employs $2^N$ power amplifiers (PAs) illustrated as ideal voltage sources in this figure for analysis purposes. The power combiner is ideally lossless, and comprises reactive elements with specified impedances at the operating frequency. The combiner has $2^N$ power amplifier input ports and one power output port for the load $R_L$.

## B.2. Effective Input Admittances

To characterize the behavior of the power combiner system, one must examine the effective admittance seen by each source for the stipulated input-port voltage phasor relationships (B1). The effective admittance at a combiner input port is the complex ratio of current to voltage at the port with all sources active. The effective admittances represent the admittances "seen" by the sources when they are operating under outphasing control [29]. The exact expressions for the effective admittances depend on the specific number of stages in the power combiner. Nevertheless, this sub-section presents a general analysis technique which offers valuable insight in understanding the behavior of the input admittances over the operating power range.

Consider the N-stage power combining system of Fig. B-1 and its dual RCN of Fig. A-1, and let the respective reactance magnitudes be equal (i.e. $|X_1|$ in the combiner is equal to $|X_1|$ in the RCN, etc.). Suppose that the load resistance $R_o$ in the RCN is set to a value that will force the input resistance $R_{in,N}$ to $R_{in,N,med}$ (this corresponds to any of the intersection points in Fig. A-2). Further, suppose that $R_L$ in the power combiner is equivalent to $R_{in,N,med}$ in the RCN, and let the outphasing control angles be selected according to (A7), i.e. the voltages at the combiner input terminals are equivalent to the respective voltages across the $R_o$ loads in the RCN network. In this scenario, the power combiner is a perfect dual of the RCN (RCN node voltages are equal to the respective combiner node voltages, while RCN branch currents are the negative of the respective combiner branch currents). As a result, the effective input impedance of each input port of the power combiner is entirely resistive and equal to $R_o$. This is also the case for any of the $2^N$ intersection points in Fig. A-2. This leads to an important observation: for a given $R_L$, an N-stage power combiner will exhibit entirely resistive effective input admittances on all of its input ports for exactly $2^N$ distinct combiner output power levels. Since the phases associated with the effective input admittances at these power levels are identically zero, the operating points corresponding to these power levels are termed here the *zero-points*. It is important to mention that at a zero-point, the sourced currents $I_1 - I_{2^N}$ (see Fig. B-1) are in phase with the input voltages $V_1 - V_{2^N}$ and given by:

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{2^N} \end{bmatrix} = \frac{V_S}{r_o} \begin{bmatrix} e^{j\varphi_1} \\ e^{j\varphi_2} \\ \vdots \\ e^{j\varphi_{2^N}} \end{bmatrix} \tag{B2}$$

Suppose now that it is desired to operate at another power level (not a zero-point). First compute the resistive PA loading $r_{o,new}$ that corresponds to the selected combiner output power level $P_{out}$ based on the PA drive amplitude $V_S$ and the $2^N$- number of PAs (B3).

$$r_{o,new} = \frac{V_S^2}{2} \Big/ \frac{P_{out}}{2^N} \tag{B3}$$

Let the new input impedance of the dual RCN with $R_o = r_{o,new}$ be $R_{in,N,new}$. Clearly, if the load $R_L$ of the power combiner changes to $R_{in,N,new}$, then it would establish a new zero-point. However, in practical applications, $R_L$ is fixed and determined by the actual load that one is driving. Nevertheless, this fact can be modeled by incorporating an incremental resistance of $\Delta R_L = R_L - R_{in,N,new}$ in series with $R_{in,N,new}$ thus preserving a total resistance of $R_L$. Next, the Alternation Theorem [56] can be employed to asses the effect of $\Delta R_L$ on the input currents $I_1 - I_{2^N}$ provided by each power amplifier (see Fig. B-1). According to the Alternation Theorem, the resulting incremental currents $\Delta I_1 - \Delta I_{2^N}$ can be determined by analyzing the network in Fig. B-2, where $I_L$ is the zero-point load current that would flow through $R_L$ if $\Delta R_L = 0$ (i.e. if

$R_L$ actually changes to $R_{in,N,new}$). Although Fig. B-2 presents only part of the N-stage combiner network in Fig. B-1, it is sufficient the analysis purposes here and the obtained results are valid in general.

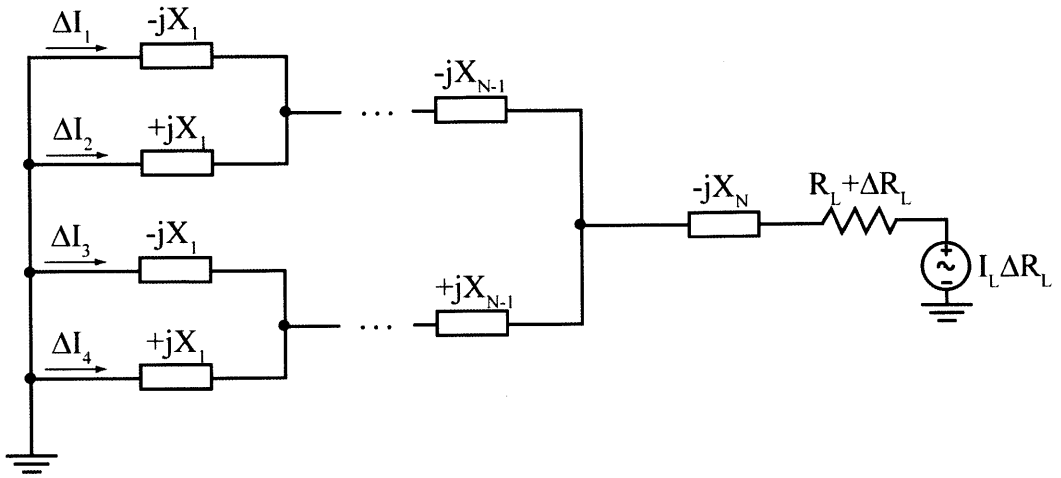



Fig. B-2: Network utilized for analyzing the incremental change of sourced input currents by the power amplifiers (Fig. B-1) for a given incremental change in load resistance $R_L$ by employing the Alternation Theorem [56]. $I_L$ is the load current in Fig. B-1 when $\Delta R_L=0$.

By employing conventional linear circuit analysis techniques, it is readily shown that the incremental currents are given by (B4):

$$\Delta I_n = \pm j\frac{I_L \Delta R_L}{X_1} = \pm j\frac{R_L - R_{in,N,new}}{X_1}\sqrt{\frac{2P_{cmd}}{R_{in,N,new}}} \quad \text{for } 1 \le n \le N \tag{B4}$$

where the sign is selected depending on the nature of the reactive element $X_1$: (+) for inductive elements, and (-) for capacitive elements.

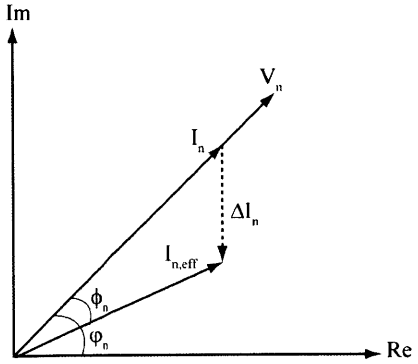



Fig. B-3: Phasor plot of the effective current $I_{n,eff}$ sourced by a particular power amplifier of Fig. B-1 for a given combiner output power level.

Fig. B-3 illustrates how such a current increment $\Delta I_n$ can phase-offset the zero-point current $I_n$ (the current that would be sourced by a particular power amplifier in Fig. B-1 if $R_L$ changes to $R_{in,N,new}$), and as a result, introduce an effective input impedance phase of $\phi_n$. $V_n$ is the voltage of the particular amplifier with a desired outphasing control angle of $\varphi_n$. Note that by choosing a smaller k-value for the

combiner/RCN network design (see RCN design, Appendix A), one can reduce variations of $R_{in,N,new}$ about $R_L$, and thus decrease the effective input impedance phases. However, as will be demonstrated, smaller k-values are associated with limiting the power operating range of the power combiner.

## B.3. Output Power Control

First, consider the combiner of Fig. B-1 operating at a particular zero-point characterized with a "commanded" power level $P_{cmd}$. The "commanded" power is the output power level that one wishes the combiner to deliver to its load based on which the outphasing control angles are selected. As already demonstrated in the previous section, the effective input impedance $r_o$ "seen" by each PA driving the combiner is entirely resistive at a zero-point. The resultant output power $P_{out}$ supplied by all amplifiers to the load $R_L$ is given by (B5) and is equivalent to $P_{cmd}$.

$$P_{out} = P_{cmd} = \frac{2^{N-1} V_S^2}{r_o}. \tag{B5}$$

Suppose now that one decides to operate the combiner at a $P_{cmd}$ not associated with a zero-point. Then it can be shown that due to the resultant purely-imaginary incremental offset $\Delta I_n$ to the zero-point current sourced by a particular amplifiers (B4), the power it supplies to the load is given by (B6) where $V_s$ is the amplitude of the voltage of each power amplifier and $\varphi_n$ is its respective outphasing control angle. Therefore, the total output power delivered to the load $R_L$ for a given $P_{cmd}$ can be expressed by (B7).

$$P_{out,n} = \frac{1}{2} Re\{V_n I_{n,eff}^*\} = \frac{1}{2} Re\{V_n (I_n + \Delta I_n)^*\} = \frac{P_{cmd}}{2^N} + \frac{\Delta I_n V_s}{2j} sin(\varphi_n) \tag{B6}$$

$$P_{out} = \sum_{n=1}^{2^N} P_{out,n} = P_{cmd} + \sum_{n=1}^{2^N} \frac{\Delta I_n V_s}{2j} sin(\varphi_n) \tag{B7}$$

Selecting a sufficiently small design k-value reduces $\Delta I_n$ and as a result can decrease the deviation between $P_{out}$ and $P_{cmd}$ to an arbitrary amount. However, as already mentioned, this adversely affects the power operating range. Nevertheless, the relationship between $P_{out}$ and $P_{cmd}$ (B7) is a monotonic function, and nonlinearities can be readily addressed through predistortion or other means [29].

## B.4. The Eight-Way Power Combiner

This sub-section summarizes some key characteristics of the eight-way combiner. One possible implementation this combiner (the "binary-tree" implementation) is shown in Fig. B-4. The effective

admittance matrix $Y_{eff}$ relating the input currents to the source voltages of the above network is given by (B8)-(B11) where $\alpha = X_2/X_1$, $\beta = X_3/X_1$ and $\gamma = R_L/X_1$.

$$Y_{eff} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \tag{B8}$$

$$M_{11} = \begin{bmatrix} \gamma + j(\alpha+\beta-1) & -\gamma - j(\alpha+\beta) & \gamma + j\beta & -\gamma - j\beta \\ -\gamma - j(\alpha+\beta) & \gamma + j(\alpha+\beta+1) & -\gamma - j\beta & \gamma + j\beta \\ \gamma + j\beta & -\gamma - j\beta & \gamma - j(\alpha-\beta+1) & -\gamma + j(\alpha-\beta) \\ -\gamma - j\beta & \gamma + j\beta & -\gamma + j(\alpha-\beta) & \gamma - j(\alpha-\beta-1) \end{bmatrix} \tag{B9}$$

$$M_{12} = M_{21} = \begin{bmatrix} \gamma & -\gamma & \gamma & -\gamma \\ -\gamma & \gamma & -\gamma & \gamma \\ \gamma & -\gamma & \gamma & -\gamma \\ -\gamma & \gamma & -\gamma & \gamma \end{bmatrix} \tag{B10}$$

$$M_{22} = \begin{bmatrix} \gamma - j(\beta-\alpha+1) & -\gamma + j(\beta-\alpha) & \gamma - j\beta & -\gamma + j\beta \\ -\gamma + j(\beta-\alpha) & \gamma - j(\beta-\alpha-1) & -\gamma + j\beta & \gamma - j\beta \\ \gamma - j\beta & -\gamma + j\beta & \gamma - j(\alpha+\beta+1) & -\gamma + j(\alpha+\beta) \\ -\gamma + j\beta & \gamma - j\beta & -\gamma + j(\alpha+\beta) & \gamma - j(\alpha+\beta-1) \end{bmatrix} \tag{B11}$$

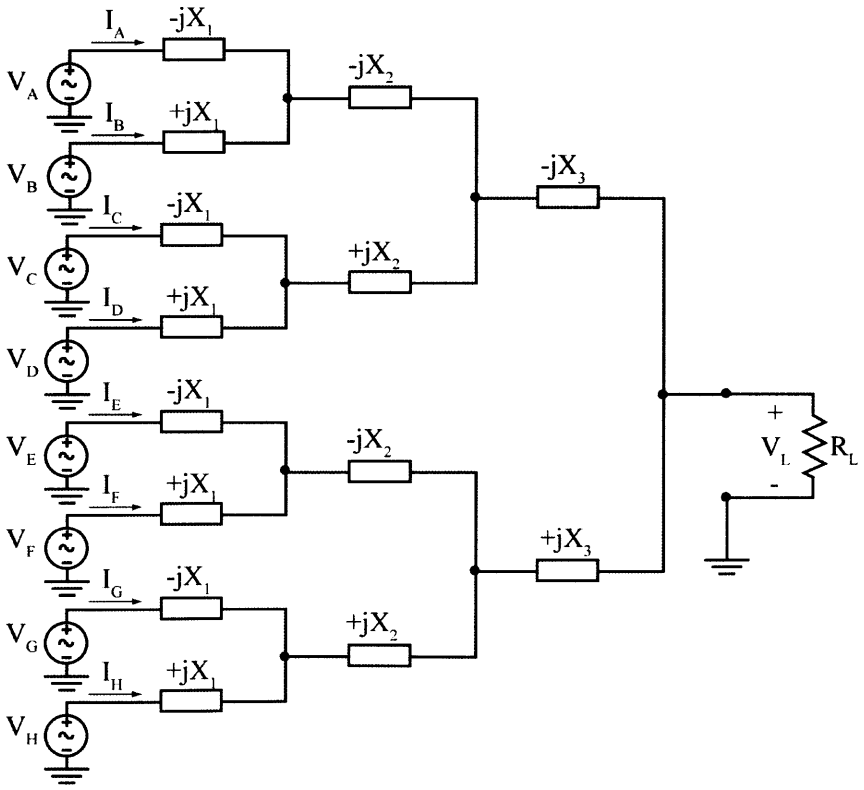



Fig. B-4: An example implementation of a three-stage power combiner

The PAs driving the combiner are outphased according to (B12) with Fig. B-5 depicting a phasor representation of the combiner input-port terminal voltages.

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \\ V_E \\ V_F \\ V_G \\ V_H \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta}e^{-j\psi} \\ e^{+j\phi}e^{-j\theta}e^{-j\psi} \\ e^{-j\phi}e^{+j\theta}e^{-j\psi} \\ e^{+j\phi}e^{+j\theta}e^{-j\psi} \\ e^{-j\phi}e^{-j\theta}e^{+j\psi} \\ e^{+j\phi}e^{-j\theta}e^{+j\psi} \\ e^{-j\phi}e^{+j\theta}e^{+j\psi} \\ e^{+j\phi}e^{+j\theta}e^{+j\psi} \end{bmatrix}. \quad \text{(B12)}$$

Although the effective input admittance seen at each port of the power combiner can be derived similarly to the case of the four-way combiner (Chapter 2), the exact expressions are omitted here due to their complexity and large number of terms. Nevertheless, it is important to note that the effective input admittances seen at the ports A and H, B and G, C and F, D and E are complex conjugate pairs (see Fig 2-14).

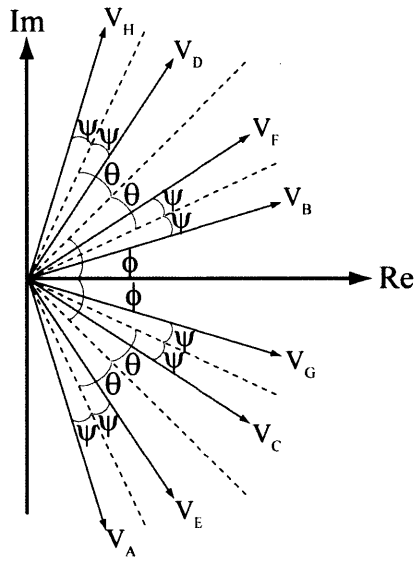



Fig. B-5: Phasor diagram showing the relationship among the phase voltages for a three-stage power combiner. The outphasing control angles $\phi$, $\theta$ and $\psi$ are used to regulate output power while maintaining desirable loading of the sources A-H.

Various outphasing control methodologies (OP, OS, and IRCN) were presented in Chapter 2 for controlling the output power of a four-way combiner. These methodologies are also applicable to the case of the eight-way combiner, although deriving the exact control angle expressions is a laborious procedure. Of course, for any particular eight-way combiner design, the OP, OS, or IRCN control angles can be computed numerically by simply sweeping the control angles over the range [0 to 180°] and selecting only the control angle pairs which yield the desired combiner input admittance characteristics. Although a MATLAB script that performs this operation can be easily created, another outphasing control methodology is instead presented hear which results in combiner input admittance characteristics similar to

those of OP, OS and IRCN control. This new control strategy, termed approximate inverse RCN control (AIRCN) entails outphasing the PAs according to (A17)-(A19) with $R_o = 4V_S^2/P_{cmd}$, where $P_{cmd}$ is the commanded combiner power - the output power that one desires the combiner do deliver to its load. Essentially, this control strategy aims to drive the input ports of the combiner with voltage waveforms that are a replica of the voltages measured across the $R_o$ loads in the corresponding three-stage RCN network. As was already discussed, the combiner network is not a true inversion of the RCN network, and hence this outphasing control methodology inevitably results in a certain mismatch between the commanded power $P_{cmd}$ and the actual combiner output power $P_{out}$. The outphasing AIRCN control angles and the resultant $P_{cmd}$-$P_{out}$ characteristic are respectively shown in Fig. B-6 and Fig. B-7 for an example design of an eight-way combiner with $V_s = 1$ V, $R_L = 50\ \Omega$, $X_1 = 18.13\ \Omega$, $X_2 = 42.29\ \Omega$ and $X_3 = 49.68\ \Omega$. Furthermore, Fig. B-8 and Fig. B-9 show its input admittance characteristics. Note that in an actual power combining system, the mismatch between the commanded and the output power can be addressed easily by simply pre-distorting the outphasing control - an approach widely used in many contemporary power amplification systems. Similarly to the case of the four-way combiner, the conductive loading of the PA modulates in accordance with output power, while susceptive (and phase) variations are limited to certain peak value.

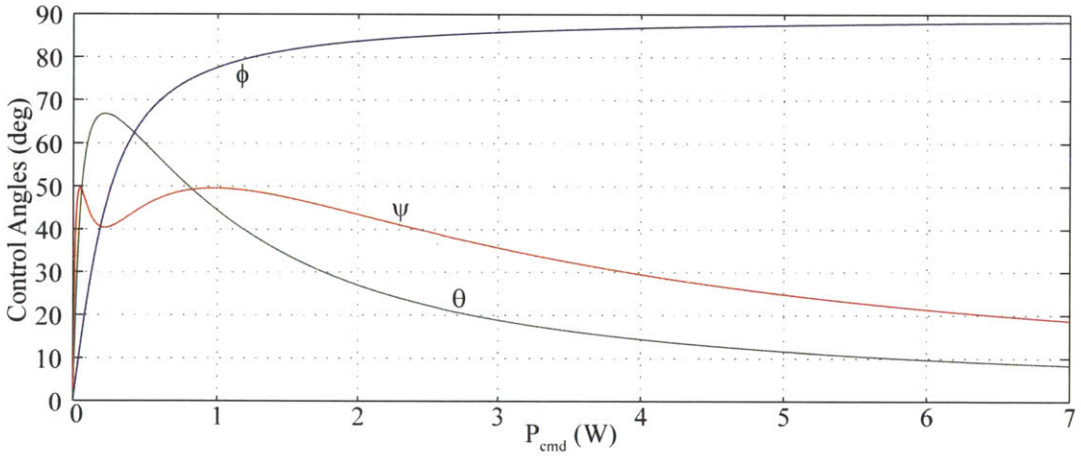



Fig. B-6: Plot showing the outphasing control angles $\phi$, $\theta$ and $\psi$ versus commanded output power $P_{cmd}$ according to (48) for the three-stage power combiner example design ($V_s = 1$ V, $R_L = 50\ \Omega$, $X_1 = 18.13\ \Omega$, $X_2 = 42.29\ \Omega$ and $X_3 = 49.68\ \Omega$).

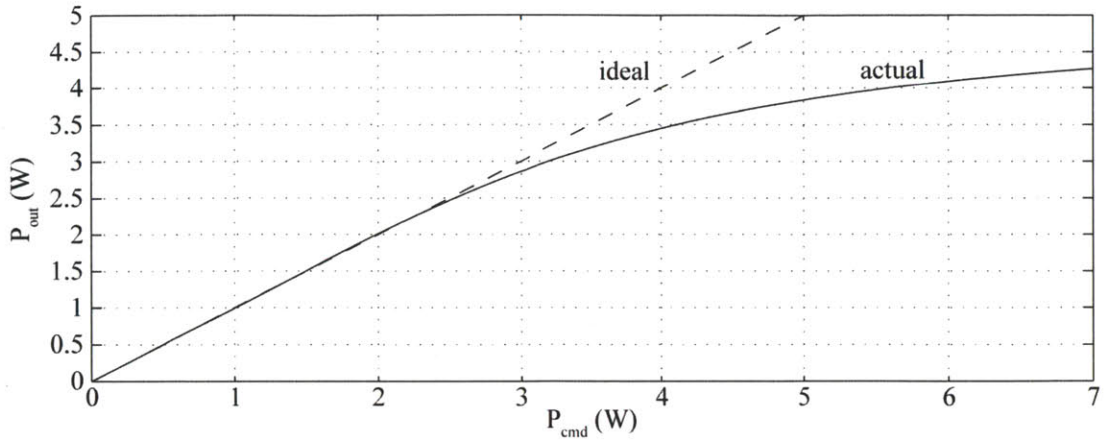



Fig. B-7: Actual output power versus commanded power for the three-stage power combiner example design ($V_s$ = 1 V, $R_L$ = 50 Ω, $X_1$ = 18.13 Ω, $X_2$ = 42.29 Ω and $X_3$ = 49.68 Ω). The actual power increases monotonically with $P_{cmd}$ and saturates at approximately 4.5 W for higher commanded power levels.

It is readily observable from Fig. B-8 and Fig. B-9 that the three-stage combiner has exactly eight zero-points associated with purely conductive input effective admittances (phase is zero). Moreover, if the maximum effective admittance phase is constrained to 5°, this design allows one to operate over an approximate output power range of [0.02 W, 3.5 W], or an output power range ratio of 22.4 dB (compared to approximately 12 dB for a four-way combiner).

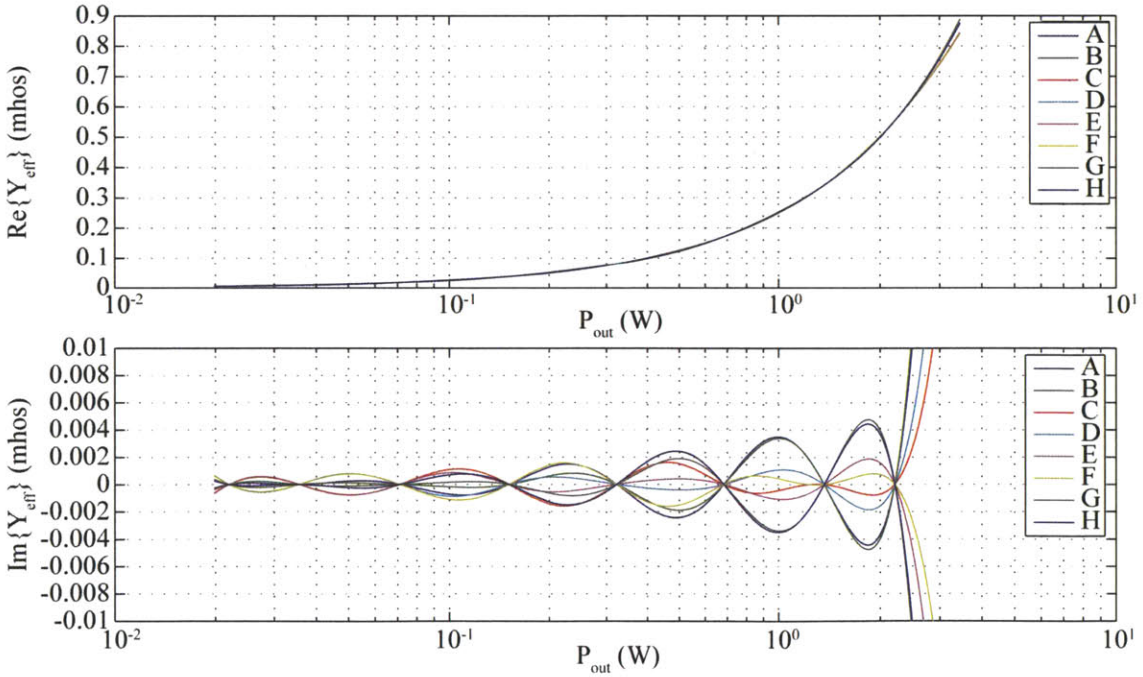



Fig. B-8: Real and imaginary components of the effective admittances seen at each of the power combiner input ports (A-H) plotted as a function of actual output power $P_{out}$. The plots are shown for the three-stage combiner example ($V_s$ = 1 V, $R_L$ = 50 Ω, $X_1$ = 18.13 Ω, $X_2$ = 42.29 Ω and $X_3$ = 49.68 Ω).

The k-value selection methodology presented in Chapter 2 is also adopted for the design of the eight-way combiner (Fig. B-11 and Fig. B-12) Assuming $V_S$ = 1 V and $R_L$ = 1 Ω, the obtained results in this section can be de-normalized for any particular $V_S$ and $R_L$ by simply scaling all power levels by $V_S^2/R_L$, and all impedances by $R_L$. Fig. B-10 shows the maximum absolute value of the phases associated with the effective input admittances at the input ports of the eight-way combiner for various $k$-values versus the output power ranges. Similar to the four-way power combiner, it can be observed that although smaller $k$ values result in overall smaller admittance phases, the operating power range is reduced. Also note that, in contrast to the four-way combiner, the eight-way combiner has exactly eight zero-points.

Fig. 2-24 provides the design curves for the eight-way combiner which illustrate respectively the largest obtainable output power range ratio for a given maximum admittance phase constraint and indicate the corresponding $k$-value. The performance advantage of the eight-way combiner over that of the four-way combiner (from the standpoint of the most resistive PA loading achievable) is obvious. For example, if one demands an operating power range ratio of 20 dB, an amplifier driving the eight-way combiner may see a maximum admittance phase of approximately 3°, while an amplifier driving the four-way combiner with the same PRR will observe a worst-case admittance phase of over 50° (see Fig. 2-12). After the appropriate $k$-value has been selected, the expression in (A6) is applied to calculate the necessary reactances in the combiner. The normalized limits of the operating output power range for each value of $k$ for the eight-way combiner is plotted in Fig. B-12.

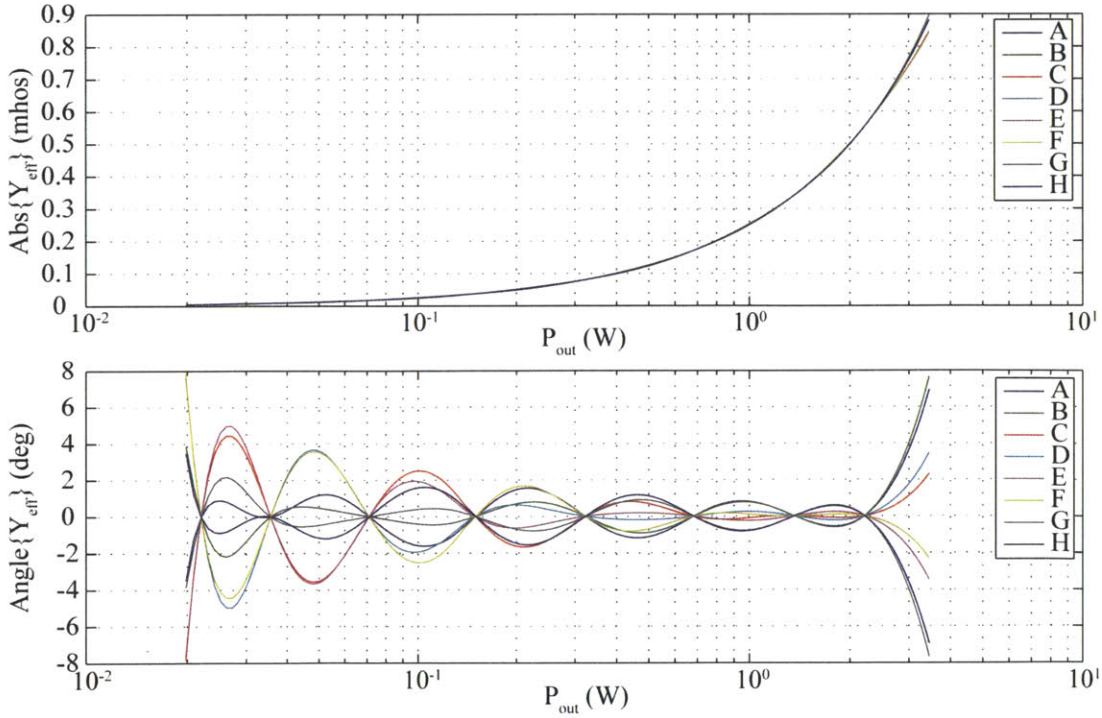



Fig. B-9: Magnitude and phase of the effective admittances seen at each of the power combiner input ports (A-H) plotted as a function of actual output power $P_{out}$. The plots are shown for the two-stage combiner example ($V_s$ = 1 V, $R_L$ = 50 Ω, $X_1$ = 18.13 Ω, $X_2$ = 42.29 Ω and $X_3$ = 49.68 Ω).

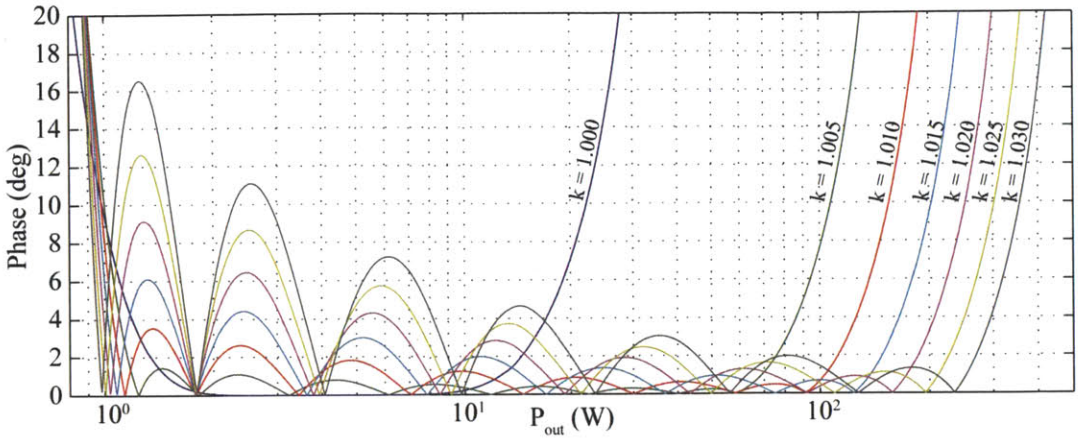



Fig. B-10: Absolute value of the maximum effective input admittance phase seen at the input ports of a two-stage (top) and three-stage (bottom) power combiners versus the output power level for various k-values. The plot is normalized to $V_S = 1$ V and $R_L = 1\ \Omega$; denormalize for a particular $V_S$ and $R_L$ by scaling the $P_{out}$ axis by $V_S^2 / R_L$.

Although so far only the "binary-tree" implementation of the eight-way combiner, just as in the case of the four-way combiner, various topological transformations may be carried-out on the original combiner implementation of Fig. B-4. Fig. B-13 shows the "binary-tree"-implementation of an eight-way combiner along with outlined component groups over which a T-Δ transformation may be applied, and Fig. B-14 illustrates the respective incremental loss curves. Again, similarly to the transformations considered in the four-way combiner, only transformations that do not involve common components may be performed simultaneously – two α-transformations along with two β-transformations and a δ-transformation preclude γ-transformations.

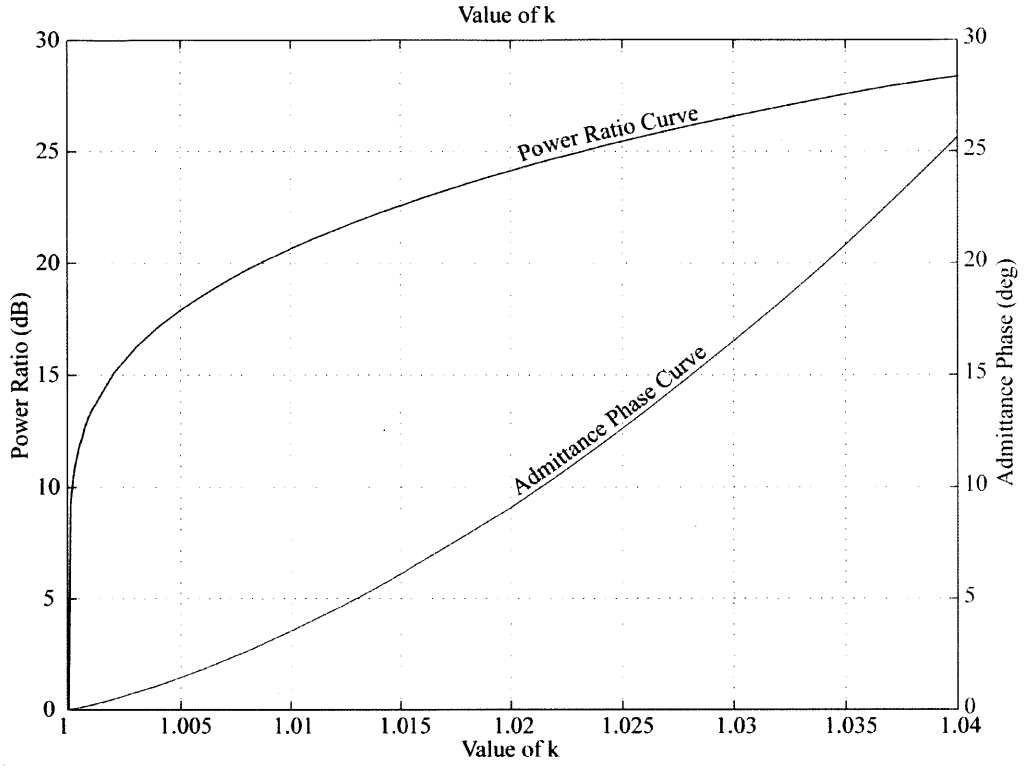



Fig. B-11: Design curves for the two-stage (top) and three-stage (bottom) power combiners: trace-out the desired operating output power range ratio to the Power Ratio Curve to determine the appropriate design value for k. The Admittance Phase Curve gives the corresponding worst-case effective input admittance phase that may be seen over the entire operating range at the input ports of the combiner.

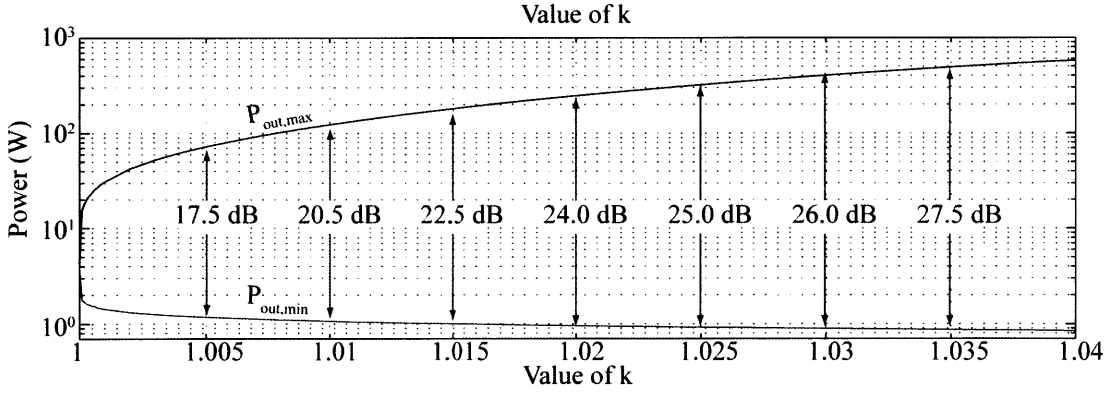



Fig. B-12: Normalized plot ($V_S$ = 1 V, $R_L$ = 1 Ω) of the minimum and maximum limits of the output power operating range versus the k-value for a two-stage (top) and a three-stage (bottom) power combiners. To denormalize for a particular $V_S$ and $R_L$, multiply the power axes by $v_S^2/R_L$.

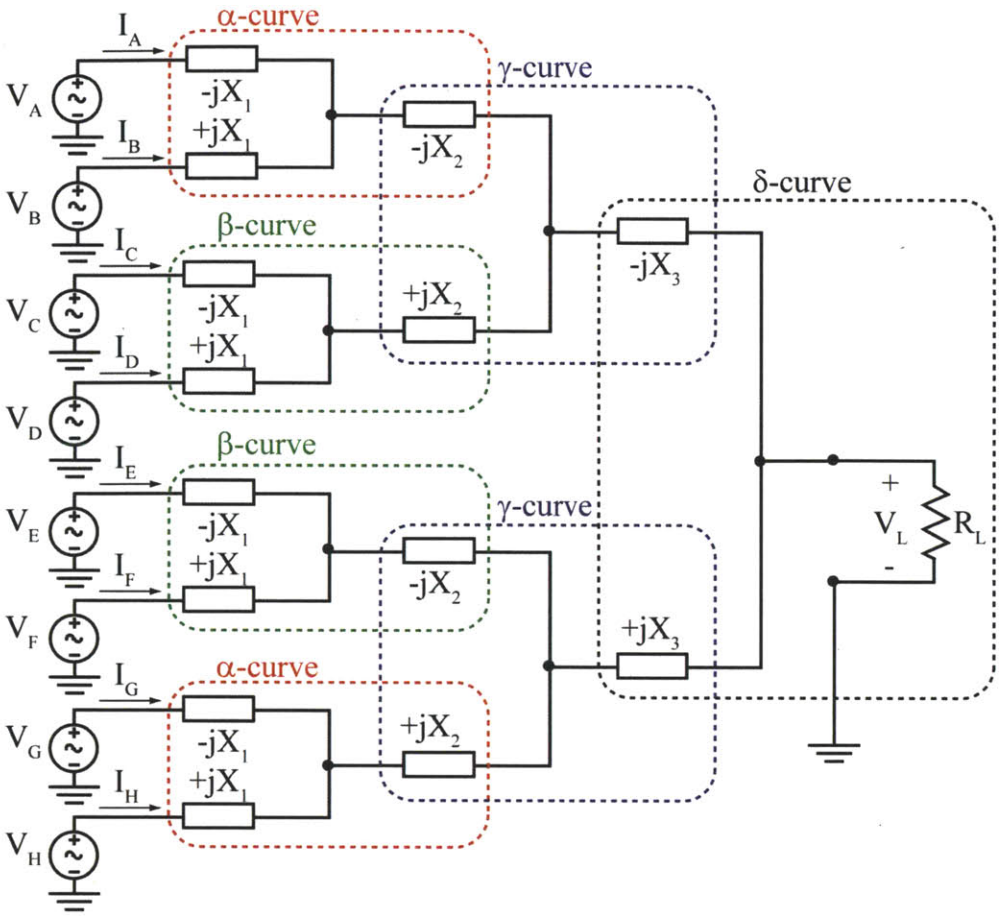



Fig. B-13: Basic T-network implementation of a three-stage power combiner along with outlined possible topological transformations and their corresponding incremental fractional loss curves in Fig. B-14.

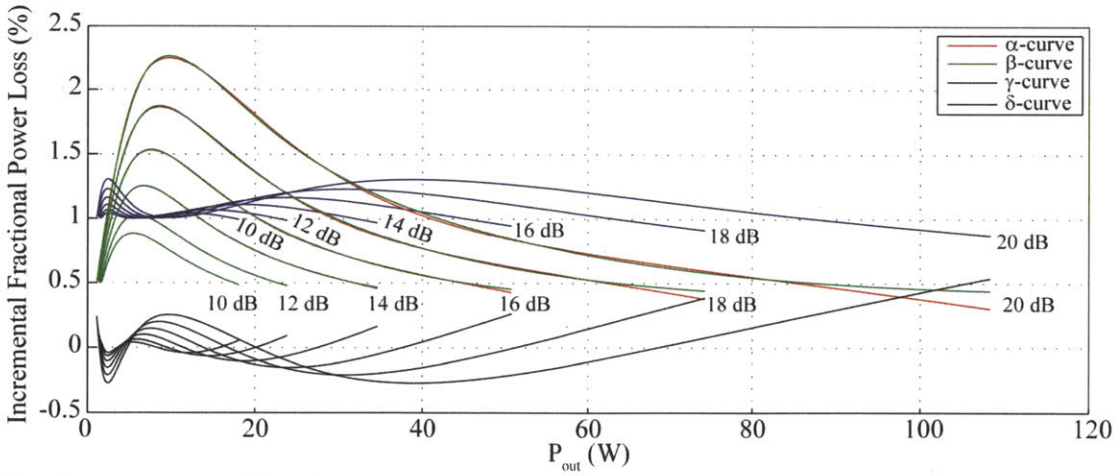



Fig. B-14: Incremental fractional power loss curves for a three-stage power combiner for various operating power range ratios. $P_{out}$ is normalized to $R_L = 1\ \Omega$ and $V_S = 1$ V.

## Appendix C

# MATLAB Code

combiner4_outphasing_control.m

```
% ------------------------------------------------------------------------
% Description:
% ------------------------------------------------------------------------
% Compute the Optimal-Susceptance (OS), Optimal-Phase (OP) and Inverse
RCN
% (IRCN) control angles for a four-way combiner, and plot the resultant
% combiner effective input admittances over its operating output power
% range
% ------------------------------------------------------------------------

close all;
clear all;
clc;

% Design Parameters
RL = 50;            % Combiner Load (ohm)
Vs = 25;            % PA voltage drive amplitude (V)
k = 1.042;          % Combiner design factor (obtained from design
charts)

% Compute Combiner Reactances
X2 = 2*RL/(k+1);              % Stage 2 reactance (Closest to Load)
X1 = X2/(k+sqrt(k^2-1));      % Stage 1 reactance (Closest to PA)
c = RL/X1;
b = X2/X1;

% Compute Admittance Matrix
Y_MX = [c+j*(1-b), -c+j*b, c, -c;
        -c+j*b, c-j*(b+1), -c, c;
        c, -c, c+j*(b+1), -c-j*b;
        -c, c, -c-j*b, c+j*(b-1)]/X1;

Psat = 8*RL*Vs^2/X1^2;          % Output power saturation level
Pout = [0:0.001:0.9]*Psat;      % Output Power Range
phi = [0:0.00001:1]*pi/2;         % phi sweep range

% Result Arrays
min_phase = zeros(1, length(Pout));
min_phi_phase = zeros(1, length(Pout));
min_theta_phase = zeros(1, length(Pout));
yeff_optim_phase = zeros(4, length(Pout));

min_imag = zeros(1, length(Pout));
min_phi_imag = zeros(1, length(Pout));
min_theta_imag = zeros(1, length(Pout));
yeff_optim_imag = zeros(4, length(Pout));
```

```
% Exhaustive Search for the Optimal Control Angles
for n=1:length(Pout)
    % Compute corresponding theta for a given Pout
    theta = acos(sqrt(X1^2/8/RL/Vs^2*Pout(n)./(sin(phi).*sin(phi))));

    % Select all the possible real-valued control angle pairs
    index = find(imag(theta)==0);
    phi_new = phi(index);
    theta_new = theta(index);

    % Determine Maximum Admittance Phase and Susceptance
    % for each control angle pair
    yeff_phase_max = zeros(1, length(phi_new));
    yeff_imag_max = zeros(1, length(phi_new));
    yeff = zeros(4, length(phi_new));
    for m=1:length(phi_new)
        Vin = Vs*[exp(j*(-phi_new(m)-theta_new(m)));exp(j*(phi_new(m)-
theta_new(m)));
                  exp(j*(-
phi_new(m)+theta_new(m)));exp(j*(phi_new(m)+theta_new(m)))];
        Iin = Y_MX*Vin;
        yeff(:,m) = Iin./Vin;
        yeff_phase_max(m) = max(abs(angle(yeff(:,m))));
        yeff_imag_max(m) = max(abs(imag(yeff(:,m))));
    end

    % Store the optimal-phase control angle pairs
    [min_phase(n), min_index] = min(yeff_phase_max);
    min_phi_phase(n) = phi_new(min_index);
    min_theta_phase(n) = theta_new(min_index);
    yeff_optim_phase(:,n)=yeff(:,min_index);

    % Store the optimal-susceptance control angle pairs
    [min_imag(n), min_index] = min(yeff_imag_max);
    min_phi_imag(n) = phi_new(min_index);
    min_theta_imag(n) = theta_new(min_index);
    yeff_optim_imag(:,n)=yeff(:,min_index);

    display(Pout(n));
end

% Compute IRCN control angles
a_coef = 1;
b_coef = 4*X2^2+2*X1^2-8*RL*Vs^2./Pout;
c_coef = X1^4-8*RL*Vs^2*X1^2./Pout;
Ro_rcn = sqrt((-b_coef+sqrt(b_coef.^2-4*a_coef.*c_coef))./(2*a_coef));
theta_rcn = atan(2*Ro_rcn*X2./(Ro_rcn.*Ro_rcn+X1^2));
phi_rcn = atan(X1./Ro_rcn);
phase_rcn = zeros(1, length(Pout));
imag_rcn = zeros(1, length(Pout));
yeff_rcn = zeros(4, length(Pout));

for m=1:length(Pout)
    Vin = Vs*[exp(j*(-phi_rcn(m)-theta_rcn(m)));exp(j*(phi_rcn(m)-
```

```
theta_rcn(m)));
                exp(j*(-
phi_rcn(m)+theta_rcn(m)));exp(j*(phi_rcn(m)+theta_rcn(m)))];
    Iin = Y_MX*Vin;
    yeff_rcn(:,m)=Iin./Vin;
    phase_rcn(m) = max(abs(angle(Iin./Vin)));
    imag_rcn(m) = max(abs(imag(Iin./Vin)));
end

% Plot OS input admittance characteristic
figure;
title('OS');
subplot(3,1,1)
plot(10*log10(Pout/100), real(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
subplot(3,1,2)
plot(10*log10(Pout/100), imag(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Susceptance (mho)');
grid on;
subplot(3,1,3)
plot(10*log10(Pout/100), 180/pi*angle(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Phase (deg)');
grid on;

% Plot OP input admittance characteristic
figure;
title('OP');
subplot(3,1,1)
plot(10*log10(Pout/100), real(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
subplot(3,1,2)
plot(10*log10(Pout/100), imag(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Susceptance (mho)');
grid on;
subplot(3,1,3)
plot(10*log10(Pout/100), 180/pi*angle(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Phase (deg)');
grid on;

% Plot IRCN input admittance characteristic
figure;
title('IRCN');
subplot(3,1,1)
plot(10*log10(Pout/100), real(yeff_rcn));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
subplot(3,1,2)
```

```
plot(10*log10(Pout/100), imag(yeff_rcn));
xlabel('Pout (dBW)');
ylabel('Susceptance (mho)');
grid on;
subplot(3,1,3)
plot(10*log10(Pout/100), 180/pi*angle(yeff_rcn));
xlabel('Pout (dB)');
ylabel('Phase (deg)');
grid on;

% Compare IRCN, OP, and OS
figure;
subplot(2,1,1)
plot(10*log10(Pout/100), 180/pi*max(abs(angle(yeff_rcn))), ...
     10*log10(Pout/100), 180/pi*max(abs(angle(yeff_optim_phase))), ...
     10*log10(Pout/100), 180/pi*max(abs(angle(yeff_optim_imag))));
xlabel('Pout (dB)');
ylabel('Maximum Admittance Phase (deg)');
legend('IRCN', 'OP', 'OS');
grid on;
subplot(2,1,2)
plot(10*log10(Pout/100), max(abs(imag(yeff_rcn))), ...
     10*log10(Pout/100), max(abs(imag(yeff_optim_phase))), ...
     10*log10(Pout/100), max(abs(imag(yeff_optim_imag))));
xlabel('Pout (dB)');
ylabel('Maximum Susceptance (S)');
legend('IRCN', 'OP', 'OS');
grid on;

% Plot Control Angles
figure;
plot(10*log10(Pout/100), 180/pi*min_phi_imag, 10*log10(Pout/100),
180/pi*min_theta_imag, ...
     10*log10(Pout/100), 180/pi*min_phi_phase, 10*log10(Pout/100),
180/pi*min_theta_phase, ...
     10*log10(Pout/100), 180/pi*phi_rcn, 10*log10(Pout/100),
180/pi*theta_rcn);
 xlabel('Pout (W)');
 ylabel('Outphasing Control Angles (deg)');
 grid on;
```

combiner4_design_curves.m

```
% ------------------------------------------------------------------------
% Description:
% ------------------------------------------------------------------------
% Compute the design curves and the zero-point output power levels
% for the four-way combiner
% ------------------------------------------------------------------------

close all;
clear all;
clc;

RL = 1;          % Combiner Load
Vs = 1;          % PA voltage amplitude
k = [1:0.001:1.3];      % Design factor range

max_phase_ircn = [];  % peak phase for a given k-value with IRCN
control
max_phase_os = [];    % peak phase for a given k-value with OP/OS
control
max_sscpt_ircn = [];  % peak susceptance for a given k-value with IRCN
control
max_sscpt_os = [];    % peak susceptance for a given k-value with OP/OS
control
p_zero_points = [];   % zero-point power levels (four zero-points per
k-value)
prr = [];             % power-range ratio for a given k-value


for n=1:length(k)

    X2 = 2*RL/(k(n)+1);               % Stage 2 reactance (Closest to
Load)
    X1 = X2/(k(n)+sqrt(k(n)^2-1));    % Stage 1 reactance (Closest to
PA)
    c = RL/X1;
    b = X2/X1;

    Y_MX = [c+j*(1-b), -c+j*b, c, -c;
            -c+j*b, c-j*(b+1), -c, c;
            c, -c, c+j*(b+1), -c-j*b;
            -c, c, -c-j*b, c+j*(b-1)]/X1;

    % Calculate the zero-points
    var1 = sqrt(RL^2-X2^2);
    var2 = 2*RL^2-X1^2-X2^2;
    var3 = (2*RL^3-2*RL*X2^2)/var1;

    pz1 = 2*Vs^2/(RL+var1-sqrt(var2+var3));
    pz2 = 2*Vs^2/(RL+var1+sqrt(var2+var3));
    pz3 = 2*Vs^2/(RL-var1-sqrt(var2-var3));
    pz4 = 2*Vs^2/(RL-var1+sqrt(var2-var3));
    p_zero_points(n,:) = [pz1, pz2, pz3, pz4];
    prr(n) = 10*log10(max([pz1, pz2, pz3, pz4])/min([pz1, pz2, pz3,
```

```
pz4]));

    % Calculate effective input admittances over the range [pz1, pz2]
    Pout = linspace(pz1, pz2, 1000);

    % Compute OS/OP control angles
    theta = acos(sqrt((4*Vs^4+Pout.*Pout*X1^2)./(8*Pout*RL*Vs^2)));
    phi = atan(Pout*X1/2/Vs^2);
    % Compute Yeff with OS/OP control and store peak phase/susceptance
    for m=1:length(phi)
        Vin = Vs*[exp(j*(-phi(m)-theta(m)));exp(j*(phi(m)-theta(m)));
                  exp(j*(-phi(m)+theta(m)));exp(j*(phi(m)+theta(m)))];
        Iin = Y_MX*Vin;
        yeff(:,m) = Iin./Vin;
    end
    max_phase_os(n) = max(max(abs(angle(yeff))));
    max_sscpt_os(n) = max(max(abs(imag(yeff))));

    % Compute IRCN control angles
    a_coef = 1;
    b_coef = 4*X2^2+2*X1^2-8*RL*Vs^2./Pout;
    c_coef = X1^4-8*RL*Vs^2*X1^2./Pout;
    Ro_rcn = sqrt((-b_coef+sqrt(b_coef.^2-
4*a_coef.*c_coef))./(2*a_coef));
    theta = atan(2*Ro_rcn*X2./(Ro_rcn.*Ro_rcn+X1^2));
    phi = atan(X1./Ro_rcn);
    % Compute Yeff with IRCN control and store peak phase/susceptance
    for m=1:length(phi)
        Vin = Vs*[exp(j*(-phi(m)-theta(m)));exp(j*(phi(m)-theta(m)));
                  exp(j*(-phi(m)+theta(m)));exp(j*(phi(m)+theta(m)))];
        Iin = Y_MX*Vin;
        yeff(:,m) = Iin./Vin;
    end
    max_phase_ircn(n) = max(max(abs(angle(yeff))));
    max_sscpt_ircn(n) = max(max(abs(imag(yeff))));

end

% Plot power range curves
figure;
plot(k, p_zero_points);
xlabel('value of k');
ylabel('Normalized Output Power');
grid on;

% Plot design chart (admittance phase)
figure;
[AX,H1,H2] = plotyy(k, prr, k, [max_phase_os;max_phase_ircn]*180/pi);
xlabel('Value of k');
set(get(AX(1),'Ylabel'),'String','Power Ratio (dB)');
set(get(AX(2),'Ylabel'),'String','Admittance Phase (deg)');
grid on;

% Plot design chart (susceptance)
figure;
```

```
[AX,H1,H2] = plotyy(k, prr, k, [max_sscpt_os;max_sscpt_ircn]);
xlabel('Value of k');
set(get(AX(1),'Ylabel'),'String','Power Ratio (dB)');
set(get(AX(2),'Ylabel'),'String','Normalized Susceptance');
grid on;
```

combiner4_q_loss_v2.m

```
% ------------------------------------------------------------------------
% Description:
% ------------------------------------------------------------------------
% Evaluate the Q-loss curves for several 4-way combiners designed to
% oeprate over 10dB, 12dB, 14dB and 16dB output power range ratio (PRR)
% ------------------------------------------------------------------------

close all;
clear all;
clc;

RL = 50;              % Load Impedance
Vs = 1;               % PA voltage amplitude
Q = 100;              % Incremental Loss Q
k = [1.052, 1.095, 1.16, 1.25];       % Design Factor List

Pout_k = [];                  % Loss-free output power
pout_range_k = [];            % Limits of Pout to comply with max
admittance phase
fl_0_k = [];                  % Fractional loss of binary tree
implementation (NSE0)
fl_inc_alpha_k = [];          % Fractional Loss by alpha transform vs k
fl_inc_beta_k = [];           % Fractional Loss by beta transform vs k

for n=1:length(k)

    X2 = 2*RL/(k(n)+1);                % Stage 2 reactance (Closest to
Load)
    X1 = X2/(k(n)+sqrt(k(n)^2-1));     % Stage 1 reactance (Closest to
PA)
    c = RL/X1;
    b = X2/X1;

    % Calculate the zero-points
    var1 = sqrt(RL^2-X2^2);
    var2 = 2*RL^2-X1^2-X2^2;
    var3 = (2*RL^3-2*RL*X2^2)/var1;

    pz1 = 2*Vs^2/(RL+var1-sqrt(var2+var3));
    pz2 = 2*Vs^2/(RL+var1+sqrt(var2+var3));
    pz3 = 2*Vs^2/(RL-var1-sqrt(var2-var3));
    pz4 = 2*Vs^2/(RL-var1+sqrt(var2-var3));
    prr(n) = 10*log10(max([pz1, pz2, pz3, pz4])/min([pz1, pz2, pz3,
pz4]));

    Y_MX = [c+j*(1-b), -c+j*b, c, -c;
            -c+j*b, c-j*(b+1), -c, c;
            c, -c, c+j*(b+1), -c-j*b;
            -c, c, -c-j*b, c+j*(b-1)]/X1;

    % Define Combiner Network Loss Matrices
    % NSE0 Network:
    T0 = [1 0 0 0;
```

```
          0 1 0 0;
          1 1 0 0;
          0 0 1 0;
          0 0 0 1;
          0 0 1 1];
    W0 = T0'*[X1/Q 0 0 0 0 0;0 X1/Q 0 0 0 0;0 0 X2/Q 0 0 0;0 0 0 X1/Q 0
0;0 0 0 0 X1/Q 0;0 0 0 0 0 X2/Q]*T0;

    % Define Incremental Loss Matrices
    % -------------------------------------------------------------------
    T_del_alpha = [-X2/X1, -X2/X1; 1+X2/X1, X2/X1; -X2/X1 1-X2/X1]*[1 0
0 0;
                                                                    0 1
0 0];
    W_del_alpha = T_del_alpha'*[X1^2/X2/Q 0 0; 0 X1/Q 0; 0 0
X1/Q]*T_del_alpha;

    T_t_alpha = [1 0; 0 1; 1 1]*[1 0 0 0; 0 1 0 0];
    W_t_alpha = T_t_alpha'*[X1/Q 0 0; 0 X1/Q 0; 0 0 X2/Q]*T_t_alpha;
    W_inc_alpha = W_del_alpha-W_t_alpha;

    T_del_beta = [1-(RL/j)/X2, -(RL/j)/X2;
                  (RL/j)/X2, 1+(RL/j)/X2]*[1 1 0 0; 0 0 1 1];
    W_del_beta = T_del_beta'*[X2/Q 0;
                             0 X2/Q]*T_del_beta;
    T_t_beta = [1 0; 0 1]*[1 1 0 0; 0 0 1 1];
    W_t_beta = T_t_beta'*[X2/Q 0;
                          0 X2/Q]*T_t_beta;
    W_inc_beta = W_del_beta-W_t_beta;
    % -------------------------------------------------------------------
    Psat = 8*RL*Vs^2/X1^2;
    Pout = linspace(0,Psat,1000);
    fl_0 = zeros(1,length(Pout));
    fl_inc_alpha = zeros(1,length(Pout));
    fl_inc_beta = zeros(1,length(Pout));

    % Compute IRCN control angles
    a_coef = 1;
    b_coef = 4*X2^2+2*X1^2-8*RL*Vs^2./Pout;
    c_coef = X1^4-8*RL*Vs^2*X1^2./Pout;
    Ro_rcn = sqrt((-b_coef+sqrt(b_coef.^2-
4*a_coef.*c_coef))./(2*a_coef));
    theta = atan(2*Ro_rcn*X2./(Ro_rcn.*Ro_rcn+X1^2));
    phi = atan(X1./Ro_rcn);

    for m=1:length(Pout)
        Vin = Vs*[exp(j*(-phi(m)-theta(m)));exp(j*(phi(m)-theta(m)));
                  exp(j*(-phi(m)+theta(m)));exp(j*(phi(m)+theta(m)))];
        Iin = Y_MX*Vin;
        Pin = real(Vin'*Iin/2);

        % Compute Q-losses
        Pdav_0 = real(Iin'*W0*Iin)/2;       % Average power dissipated
by NSE0
        fl_0(m) = Pdav_0/Pin;               % Fractional Loss for NSE0
```

```
        % Compute Incremental Q-losses
        P_inc_alpha = real(Iin'*W_inc_alpha*Iin)/2;      % Incremental
average power dissipated by alpha transform
        fl_inc_alpha(m) = P_inc_alpha/Pin;               % Incremental
Fractional Loss by alpha transform
        P_inc_beta = real(Iin'*W_inc_beta*Iin)/2;        % Incremental
average power dissipated by beta transform
        fl_inc_beta(m) = P_inc_beta/Pin;                 % Incremental
Fractional Loss by beta transform

    end

    fl_0_k = [fl_0_k;fl_0];
    fl_inc_beta_k = [fl_inc_beta_k;fl_inc_beta];
    fl_inc_alpha_k = [fl_inc_alpha_k;fl_inc_alpha];

    Pout_k = [Pout_k; Pout];
    display(k(n));
end

% NORMALIZED Q-LOSS CURVES %
figure;
hold on;
for n=1:length(k)
    Pout = Pout_k(n,:);
    Psat = max(Pout);
    fl_0 = fl_0_k(n,:);
    plot(100*Pout/Psat, 100*fl_0);
end
hold off;
xlabel('% of Psat');
ylabel('Fractional Power Loss (%)');
legend(strcat('prr=', num2str(prr',3)));
grid on;

% NORMALIZED INCREMENTAL Q_LOSS CURVES
figure;
hold on;
for n=1:length(k)
    Pout = Pout_k(n,:);
    Psat = max(Pout);
    fl_inc_alpha = fl_inc_alpha_k(n,:);
    fl_inc_beta = fl_inc_beta_k(n,:);
    plot(100*Pout/Psat, 100*fl_inc_alpha,...
         100*Pout/Psat, 100*fl_inc_beta);
end
hold off;
xlabel('% of Psat');
ylabel('Incremental Fractional Power Loss (%)');
grid on;
```

combiner4_delta_RL.m

```
% ------------------------------------------------------------------------
% Description:
% ------------------------------------------------------------------------
% Plot max effective input admittance phase vs output power of a 4-way
% combiner for various resistive/reactive changes in the combiner's
load
% ------------------------------------------------------------------------

close all;
clear all;
clc;

% Design Parameters
RL0 = 50;              % Nominal Combiner Load (ohm)
Vs = 25;              % PA voltage drive amplitude (V)
k = 1.042;            % Combiner design factor (obtained from design
charts)

% Compute Combiner Reactances
X2 = 2*RL0/(k+1);                % Stage 2 reactance (Closest to Load)
X1 = X2/(k+sqrt(k^2-1));         % Stage 1 reactance (Closest to PA)

% Define full output power range
Psat = 8*RL0*Vs^2/X1^2;           % Output power saturation level
Pout = [0:0.001:0.9]*Psat;       % Output Power Range

% Compute IRCN control angles
a_coef = 1;
b_coef = 4*X2^2+2*X1^2-8*RL0*Vs^2./Pout;
c_coef = X1^4-8*RL0*Vs^2*X1^2./Pout;
Ro_rcn = sqrt((-b_coef+sqrt(b_coef.^2-4*a_coef.*c_coef))./(2*a_coef));
theta_rcn = atan(2*Ro_rcn*X2./(Ro_rcn.*Ro_rcn+X1^2));
phi_rcn = atan(X1./Ro_rcn);

% Define RL resistive variation range (in %)
RL = (1+[-5 -2.5 0 2.5 5]/100)*RL0;
max_phase  = [];

for n=1:length(RL)

    % Compute Admittance Matrix
    c = RL(n)/X1;
    b = X2/X1;
    Y_MX = [c+j*(1-b), -c+j*b, c, -c;
            -c+j*b, c-j*(b+1), -c, c;
            c, -c, c+j*(b+1), -c-j*b;
            -c, c, -c-j*b, c+j*(b-1)]/X1;

    % Evaluate max phase for every output power level
    for m=1:length(Pout)
        Vin = Vs*[exp(j*(-phi_rcn(m)-theta_rcn(m)));exp(j*(phi_rcn(m)-
theta_rcn(m)));
            exp(j*(-
```

```
phi_rcn(m)+theta_rcn(m)));exp(j*(phi_rcn(m)+theta_rcn(m)))];
        Iin = Y_MX*Vin;
        phase(m) = max(abs(angle(Iin./Vin)));
    end
    max_phase = [max_phase;phase];
end

% Plot max phase vs Pout for all RL values
figure;
title('Resistive Load Variations');
plot(10*log10(Pout/100), max_phase*180/pi);
xlabel('Pout (dB)');
ylabel('Max Admittance Phase (deg)');
legend(num2str(RL'));
grid on;

% Define RL reactive variation range (in %)
RL = (1+j*[-5 -2.5 0 2.5 5]/100)*RL0;
max_phase  = [];

for n=1:length(RL)

    % Compute Admittance Matrix
    c = RL(n)/X1;
    b = X2/X1;
    Y_MX = [c+j*(1-b), -c+j*b, c, -c;
            -c+j*b, c-j*(b+1), -c, c;
            c, -c, c+j*(b+1), -c-j*b;
            -c, c, -c-j*b, c+j*(b-1)]/X1;

    % Evaluate max phase for every output power level
    for m=1:length(Pout)
        Vin = Vs*[exp(j*(-phi_rcn(m)-theta_rcn(m)));exp(j*(phi_rcn(m)-
theta_rcn(m)));
            exp(j*(-
phi_rcn(m)+theta_rcn(m)));exp(j*(phi_rcn(m)+theta_rcn(m)))];
        Iin = Y_MX*Vin;
        phase(m) = max(abs(angle(Iin./Vin)));
    end
    max_phase = [max_phase;phase];
end

% Plot max phase vs Pout for all RL values
figure;
title('Reactive Load Variations');
plot(10*log10(Pout/100), max_phase*180/pi);
xlabel('Pout (dB)');
ylabel('Max Admittance Phase (deg)');
legend(num2str(RL'));
grid on;
```

port_param_compare.m

```
% ------------------------------------------------------------------------
% Description:
% ------------------------------------------------------------------------
% Compare the output power and input admittance characteristics of the
% ideal and implemented combiners based on the measured port-parameters
% ------------------------------------------------------------------------

clc;
close all;
clear all;

% ------------------------------------------------------------------------
% Determine the effective admittance matrix for the ideal combiner
% ------------------------------------------------------------------------
% Design Parameters
RL = 50;            % Combiner Load (ohm)
k = 1.042;          % Combiner design factor (obtained from design
charts)
Vs = 25;            % PA drive amplitude

% Compute Combiner Reactances
X2 = 2*RL/(k+1);              % Stage 2 reactance (Closest to Load)
X1 = X2/(k+sqrt(k^2-1));      % Stage 1 reactance (Closest to PA)
c = RL/X1;
b = X2/X1;

% Compute Admittance Matrix
Y_MX_1 = [c+j*(1-b), -c+j*b, c, -c;
          -c+j*b, c-j*(b+1), -c, c;
          c, -c, c+j*(b+1), -c-j*b;
          -c, c, -c-j*b, c+j*(b-1)]/X1;

% Compute OS/OP control angles
Psat = 8*RL*Vs^2/X1^2;          % Output power saturation level
Pout = (0.04:0.001:0.9)*Psat;      % Output Power Range
theta = acos(sqrt((4*Vs^4+Pout.*Pout*X1^2)./(8*Pout*RL*Vs^2)));
phi = atan(Pout*X1/2/Vs^2);
% ------------------------------------------------------------------------

% ------------------------------------------------------------------------
% Determine the effective admittance matrix for the implemented
combiner
% based the measured port-parameters
% ------------------------------------------------------------------------
% Measurement Matrix
% Z-Analyzer (AV=8, IF=300Hz, Pout=15dBm)
M = [96.50-j*308.7, 2.182+j*0.887, 4.428-j*76.83, 4.232+j*1.487, 3.621-
j*87.22;
     1.718+j*0.740, 87.76-j*246.2, 3.239-j*2.912, 6.468+j*77.97, 1.937-
j*13.70;
     3.880-j*70.04, 3.490-j*3.358, 86.70-j*280.7, 2.378+j*3.408,
2.207+j*12.45;
     3.016+j*1.156, 5.416+j*70.23, 1.755+j*2.753, 79.69-j*220.3,
4.682+j*86.55;
```

```
    4.447-j*74.31, 1.704-j*14.36, 1.822+j*11.67, 8.238+j*100.4, 85.94-
j*260.0];

 % Compute Z-parameters of combiner (treated as five-port network with
 % output being the fifth port)
 Z5x5 = zeros(size(M));
 for m=1:4
     for n=(m+1):5
         Z5x5(m,n) = sqrt((M(m,m)-M(m,n))*M(n,n));
         Z5x5(n,m) = Z5x5(m,n);
     end
     Z5x5(m,m) = M(m,m);
 end
 Z5x5(5,5) = M(5,5);

 % Determine 4x4 admittance matrix at combiner's input ports (output
 % port loaded with RL)
 RL = 50;
 Z4x4 = Z5x5(1:4,1:4)-1/(Z5x5(5,5)+RL)*[Z5x5(1,5)*Z5x5(5, 1:4);
                                        Z5x5(2,5)*Z5x5(5, 1:4);
                                        Z5x5(3,5)*Z5x5(5, 1:4);
                                        Z5x5(4,5)*Z5x5(5, 1:4)];
 Y_MX_2 = inv(Z4x4);
 % ------------------------------------------------------------------

 % Calculate the effective input admittances seen by the PAs over
operating
 % power range
 yeff1 = [];
 yeff2 = [];
 Pout1 = [];
 Pout2 = [];
 for m=1:length(phi)
     Vin = Vs*[exp(j*(-phi(m)-theta(m)));exp(j*(phi(m)-theta(m)));
               exp(j*(-phi(m)+theta(m)));exp(j*(phi(m)+theta(m)))];
     Iin = Y_MX_1*Vin;
     yeff1(:,m) = Iin./Vin;
     Pout1(m) = 0.5*real(Iin'*Vin);
     Iin = Y_MX_2*Vin;
     yeff2(:,m) = Iin./Vin;
     Pout2(m) = 0.5*real(Iin'*Vin);
 end

% Compare input admittance characteristic
figure;
subplot(2,1,1)
plot(Pout1, real(yeff1),Pout2, real(yeff2));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
legend('A','B','C','D','A_cor','B_cor','C_cor','D_cor');
subplot(2,1,2)
plot(Pout1, imag(yeff1),...
     Pout2, imag(yeff2));
xlabel('Pout (dB)');
ylabel('Susceptance (S)');
```

```
grid on;
legend('A','B','C','D','A_cor','B_cor','C_cor','D_cor');

% Compare output power characteristics
figure;
plot(Pout, Pout1, Pout, Pout2);
xlabel('Commanded Power (W)');
ylabel('Output Power (W)');
grid on;
legend('Ideal','Actual');

phi_ideal = phi;
theta_ideal = theta;
% ------------------------------------------------------------------------
% Numerically determine best OS/OP control angles for the implemented
combiner
% ------------------------------------------------------------------------
% Result Arrays
min_phase = zeros(1, length(Pout));
min_phi_phase = zeros(1, length(Pout));
min_theta_phase = zeros(1, length(Pout));
yeff_optim_phase = zeros(4, length(Pout));

min_imag = zeros(1, length(Pout));
min_phi_imag = zeros(1, length(Pout));
min_theta_imag = zeros(1, length(Pout));
yeff_optim_imag = zeros(4, length(Pout));

Pout_op = [];
Pout_os = [];

% Exhaustive Search for the Optimal Control Angles
phi = [0:0.001:1]*pi/2;          % phi sweep range
for n=1:length(phi)
    Pout_new = [];
    phi_new = phi(n);
    theta_new = [0:0.001:1]*pi/2;          % theta sweep range

    % Determine Maximum Admittance Phase and Susceptance
    % for each control angle pair
    yeff_phase_max = zeros(1, length(phi_new));
    yeff_imag_max = zeros(1, length(phi_new));
    yeff = zeros(4, length(phi_new));
    for m=1:length(theta_new)
        Vin = Vs*[exp(j*(-phi_new-theta_new(m)));exp(j*(phi_new-
theta_new(m)));
                  exp(j*(-
phi_new+theta_new(m)));exp(j*(phi_new+theta_new(m)))];
        Iin = Y_MX_2*Vin;
        yeff(:,m) = Iin./Vin;
        yeff_phase_max(m) = max(abs(angle(yeff(:,m))));
        yeff_imag_max(m) = max(abs(imag(yeff(:,m))));
        Pout_new(m) = 0.5*real(Iin'*Vin);
    end
```

```
    % Store the optimal-phase control angle pairs
    [min_phase(n), min_index] = min(yeff_phase_max);
    min_phi_phase(n) = phi_new;
    min_theta_phase(n) = theta_new(min_index);
    yeff_optim_phase(:,n)=yeff(:,min_index);
    Pout_op(n)=Pout_new(min_index);

    % Store the optimal-susceptance control angle pairs
    [min_imag(n), min_index] = min(yeff_imag_max);
    min_phi_imag(n) = phi_new;
    min_theta_imag(n) = theta_new(min_index);
    yeff_optim_imag(:,n)=yeff(:,min_index);
    Pout_os(n)=Pout_new(min_index);

    display(phi(n));
end

% Plot OS input admittance characteristic of implemented combiner after
% correcting the outphasing control angles
figure;
title('OS');
subplot(2,1,1)
plot(Pout_os, real(yeff_optim_imag));
xlabel('Pout (W)');
ylabel('Conductance (mho)');
grid on;
legend('A','B','C','D');
subplot(2,1,2)
plot(Pout_os, imag(yeff_optim_imag));
xlabel('Pout (W)');
ylabel('Susceptance (mho)');
grid on;
legend('A','B','C','D');

% Compare Ideal Control Angles with Corrected Control Angles
figure;
plot(Pout_os, 180/pi*min_phi_imag, Pout_os, 180/pi*min_theta_imag, ...
     Pout, 180/pi*phi_ideal, Pout, 180/pi*theta_ideal);
 xlabel('Pout (W)');
 ylabel('Outphasing Control Angles (deg)');
 legend('phi_cor', 'theta_cor', 'phi_id','theta_id');
 grid on;
```

combiner4_outphasing_control_TL.m

```
% Description: Determine OP and OS control angles for a transmission
line
% implementation of a four-way combiner and examine effective input
% admittance under each controll strategy
% Version 2: Maintain equal transmission line characteristic impedances

close all;
clear all;
clc;

% Design Parameters
RL = 50;            % Load Impedance
Vs = 1;             % PA voltage amplitude
k = 1.05;            % Range of Design Factor

% Compute Combiner Reactances (use them as a starting point for
computing
% TL impedances)
X2 = 2*RL/(k+1);              % Stage 2 reactance (Closest to Load)
X1 = X2/(k+sqrt(k^2-1));      % Stage 1 reactance (Closest to PA)

% Compute Transmission Line Parameters
% Design constants used with X1
delta1 = 0.01;   % Design Constant = abs(TL1_length-lambda/2)/lambda
sigma1 = 2*pi*delta1;
% Transmission Line Parameters
Z1 = X1/sin(sigma1);    % TL1 characteristic impedance (closest to PAs)
Z2 = Z1;    % TL2 characteristic impedance (closest to load)
c=RL/Z1;
b=Z2/Z1;
% Design constants used with X2
sigma2 = asin(X2/Z2);
delta2 = sigma2/2/pi;   % Design Constant = abs(TL2_length-
lambda/2)/lambda

% Compute Admittance Matrix
Y_MX = csc(sigma1)^2/Z1*[c*sec(sigma2)^2+j*(cos(sigma1)*sin(sigma1)-
b*tan(sigma2)),-c*sec(sigma2)^2+j*b*tan(sigma2),c*sec(sigma2)^2,-
c*sec(sigma2)^2; ...
                         -
c*sec(sigma2)^2+j*b*tan(sigma2),c*sec(sigma2)^2-
j*(cos(sigma1)*sin(sigma1)+b*tan(sigma2)),-
c*sec(sigma2)^2,c*sec(sigma2)^2; ...
                         c*sec(sigma2)^2,-
c*sec(sigma2)^2,c*sec(sigma2)^2+j*(cos(sigma1)*sin(sigma1)+b*tan(sigma2
)),-c*sec(sigma2)^2-j*b*tan(sigma2); ...
                         -c*sec(sigma2)^2,c*sec(sigma2)^2,-
c*sec(sigma2)^2-j*b*tan(sigma2),c*sec(sigma2)^2-
j*(cos(sigma1)*sin(sigma1)-b*tan(sigma2))];

Psat = 8*RL*Vs^2/Z1^2/sin(sigma1)^2/cos(sigma2)^2;  % Maximum output
power level
Pout = Psat*[0:0.001:0.9];                  % Output Power Range
phi = 0:0.001:pi/2;                         % Control angle phi range
```

```
% Result Arrays
min_phase = zeros(1, length(Pout));
min_phi_phase = zeros(1, length(Pout));
min_theta_phase = zeros(1, length(Pout));
yeff_optim_phase = zeros(4, length(Pout));

min_imag = zeros(1, length(Pout));
min_phi_imag = zeros(1, length(Pout));
min_theta_imag = zeros(1, length(Pout));
yeff_optim_imag = zeros(4, length(Pout));

% Exhaustive Search of the Optimal Control Angles
for n=1:length(Pout)
    % Compute corresponding theta for a given Pout
    theta =
acos(sqrt(Z1^2*sin(sigma1)^2*cos(sigma2)^2/8/RL/Vs^2*Pout(n)./(sin(phi)
.*sin(phi))));

    % Select the allowed angles only (-1<sin(phi)<1; -1<cos(theta)<1)
    index = find(imag(theta)==0);
    phi_new = phi(index);
    theta_new = theta(index);

    % Determine Maximum Admittance Phase for each control angle pair
    yeff_phase_max = zeros(1, length(phi_new));
    yeff_imag_max = zeros(1, length(phi_new));
    yeff = zeros(4, length(phi_new));
    for m=1:length(phi_new)
        Vin = Vs*[exp(j*(-phi_new(m)-theta_new(m)));exp(j*(phi_new(m)-
theta_new(m)));
                  exp(j*(-
phi_new(m)+theta_new(m)));exp(j*(phi_new(m)+theta_new(m)))];
        Iin = Y_MX*Vin;
        yeff(:,m) = Iin./Vin;
        yeff_phase_max(m) = max(abs(angle(yeff(:,m))));
        yeff_imag_max(m) = max(abs(imag(yeff(:,m))));
    end

    % Store the optimal control angle pair (the one that minimizes
    % effective input admittance phases, or susceptances)
    [min_phase(n), min_index] = min(yeff_phase_max);
    min_phi_phase(n) = phi_new(min_index);
    min_theta_phase(n) = theta_new(min_index);
    yeff_optim_phase(:,n)=yeff(:,min_index);

    [min_imag(n), min_index] = min(yeff_imag_max);
    min_phi_imag(n) = phi_new(min_index);
    min_theta_imag(n) = theta_new(min_index);
    yeff_optim_imag(:,n)=yeff(:,min_index);
    display(Pout(n));
end
```

```
% Plot OS input admittance characteristic
figure;
title('OS');
subplot(3,1,1)
plot(10*log10(Pout/0.18), real(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
subplot(3,1,2)
plot(10*log10(Pout/0.18), imag(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Susceptance (mho)');
grid on;
subplot(3,1,3)
plot(10*log10(Pout/0.18), 180/pi*angle(yeff_optim_imag));
xlabel('Pout (dB)');
ylabel('Phase (deg)');
grid on;

% Plot OP input admittance characteristic
figure;
title('OP');
subplot(3,1,1)
plot(10*log10(Pout/0.18), real(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Conductance (mho)');
grid on;
subplot(3,1,2)
plot(10*log10(Pout/0.18), imag(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Susceptance (mho)');
grid on;
subplot(3,1,3)
plot(10*log10(Pout/0.18), 180/pi*angle(yeff_optim_phase));
xlabel('Pout (dB)');
ylabel('Phase (deg)');
grid on;

% Plot Control Angles
figure;
plot(10*log10(Pout/0.18), 180/pi*min_phi_imag, 10*log10(Pout/0.18),
180/pi*min_theta_imag, ...
     10*log10(Pout/0.18), 180/pi*min_phi_phase, 10*log10(Pout/0.18),
180/pi*min_theta_phase);
 xlabel('Pout (W)');
 ylabel('Outphasing Control Angles (deg)');
 grid on;
```

combiner4_design_curves_TL.m

```
% Description: Calculate the set of design/performance curves for a
four
% way combiner
% Version 4: - Transmission line combiner implementation
%            - OS control
%            - Output power range is bound by zero-points
%            - Sweep k-value and Z2-value over a predefined range
% Last Update: July 31, 2011

close all;
clear all;
clc;

% Design Parameters
RL = 50;                % Load Impedance
Vs = 1;                 % PA voltage amplitude

% Range of k-values to explore
k = [1:0.001:1.005, 1.01, 1.02:0.02:1.24, 1.25];

% Range of Z2 values to explore (TL2 characteristic impedance)
%Z2_range = [100, 125, 150, 200, 500];
Z2_range = 500;

pout_ratio_k_delta = [];
peak_sscpt_k_delta = [];

for t=1:length(Z2_range)

    % Result Arrays
    pout_ratio_k = [];
    peak_sscpt_k = [];
    yeff_os_abs_max_k = [];
    Pout_k = [];

    for q=1:length(k)
        % -----------------------------------------------------------
        % Compute Transmission Line Parameters for given k-value
        Z2 = Z2_range(t);
        sigma2 = asin(2*RL/(k(q)+1)/Z2);       % Range of corresponding
sigma2
        delta2 = sigma2/pi/2;
        Z1 = Z2;
        X2 = Z2*sin(sigma2);              % Stage 2 reactance (Closest to
Load)
        X1 = X2/(k(q)+sqrt(k(q)^2-1));  % Stage 1 reactance (Closest to
PA)
        sigma1 = asin(X1/Z1);
        delta1 = sigma1/pi/2;
        c=RL/Z1;
        b=Z2/Z1;

        % Compute Admittance Matrix for given k
```

```
        Y_MX =
csc(sigma1)^2/Z1*[c*sec(sigma2)^2+j*(cos(sigma1)*sin(sigma1)-
b*tan(sigma2)),-c*sec(sigma2)^2+j*b*tan(sigma2),c*sec(sigma2)^2,-
c*sec(sigma2)^2; ...
            -c*sec(sigma2)^2+j*b*tan(sigma2),c*sec(sigma2)^2-
j*(cos(sigma1)*sin(sigma1)+b*tan(sigma2)),-
c*sec(sigma2)^2,c*sec(sigma2)^2; ...
            c*sec(sigma2)^2,-
c*sec(sigma2)^2,c*sec(sigma2)^2+j*(cos(sigma1)*sin(sigma1)+b*tan(sigma2
)),-c*sec(sigma2)^2-j*b*tan(sigma2); ...
            -c*sec(sigma2)^2,c*sec(sigma2)^2,-c*sec(sigma2)^2-
j*b*tan(sigma2),c*sec(sigma2)^2-j*(cos(sigma1)*sin(sigma1)-
b*tan(sigma2))];
        % ------------------------------------------------------------


        % ------------------------------------------------------------
        % Calculate zero-points
        theta_z1 = 0.5*asin(Z2*sin(2*sigma2)/2/RL); % theta
corresponding to one set of zero-points
        theta_z2 = pi/2 - theta_z1;                 % theta
corresponding to a second set of zero-points
        % polynomial for finding first set of zero-points
        poly_z1 = [Z1^2*tan(sigma1)^2*cos(sigma2)^2*cos(sigma1)^2, -
cos(theta_z1)^2*8*RL*Vs^2, 4*Vs^4*cos(sigma2)^2*cos(sigma1)^2];
        z1 = roots(poly_z1);
        index_z1 = find(imag(z1)==0);
        % polynomial for finding second set of zero-points
        poly_z2 = [Z1^2*tan(sigma1)^2*cos(sigma2)^2*cos(sigma1)^2, -
cos(theta_z2)^2*8*RL*Vs^2, 4*Vs^4*cos(sigma2)^2*cos(sigma1)^2];
        z2 = roots(poly_z2);
        index_z2 = find(imag(z2)==0);
        P_zero = [z1(index_z1)', z2(index_z2)'];
        Pmax = max(P_zero);
        Pmin = min(P_zero);
        % ------------------------------------------------------------


        % ------------------------------------------------------------
        % Determine OS control angles numerically
        Psat = 8*RL*Vs^2/Z1^2/sin(sigma1)^2/cos(sigma2)^2;  % Maximum
output power level
        Pout = linspace(Pmin, Pmax, 100);        % Output Power Range
        phi = 0:0.001:pi/2;                      % Control angle phi
range


        min_imag = zeros(1, length(Pout));
        phi_os = zeros(1, length(Pout));
        theta_os = zeros(1, length(Pout));
        yeff_os = zeros(4, length(Pout));

        for n=1:length(Pout)
            % Compute corresponding theta for a given Pout
            theta =
acos(sqrt(Z1^2*sin(sigma1)^2*cos(sigma2)^2/8/RL/Vs^2*Pout(n)./(sin(phi)
.*sin(phi))));

            % Select the allowed angles only (-1<sin(phi)<1; -
```

```
1<cos(theta)<1)
            index = find(imag(theta)==0);
            phi = phi(index);
            theta = theta(index);

            % Determine Maximum Susceptance for each control angle pair
            yeff_imag_max = zeros(1, length(phi));
            yeff = zeros(4, length(phi));
            for m=1:length(phi)
                Vin = Vs*[exp(j*(-phi(m)-theta(m)));exp(j*(phi(m)-
theta(m)));
                    exp(j*(-
phi(m)+theta(m)));exp(j*(phi(m)+theta(m)))];
                Iin = Y_MX*Vin;
                yeff(:,m) = Iin./Vin;
                yeff_imag_max(m) = max(abs(imag(yeff(:,m))));
            end

            % Store the optimal control angle pair (the one that
            minimizes
            % effective input susceptances)
            [min_imag(n), min_index] = min(yeff_imag_max);
            phi_os(n) = phi(min_index);
            theta_os(n) = theta(min_index);
            yeff_os(:,n) = yeff(:,min_index);
        end
        yeff_os_abs_max = max(abs(imag(yeff_os)));
        % ------------------------------------------------------------

        % ------------------------------------------------------------
        % Find optimum output power range for each k-value
        peaks = findpeaks(yeff_os_abs_max);
        if isempty(peaks)
            peak_sscpt = 0;
            pout_ratio = 1;
        else
            peak_sscpt = max(peaks);
            pout_ratio = Pmax/Pmin;
        end
        % ------------------------------------------------------------
        pout_ratio_k = [pout_ratio_k, pout_ratio];
        peak_sscpt_k = [peak_sscpt_k, peak_sscpt];

        k(q)
    end

    % Check the validity of the data
    % plot(Pout_k', yeff_os_abs_max_k');
    pout_ratio_k_delta = [pout_ratio_k_delta; pout_ratio_k];
    peak_sscpt_k_delta = [peak_sscpt_k_delta; peak_sscpt_k];
    Z2_range(t)
end
```

```
% DESIGN CURVES %
figure;
[AX,H1,H2] = plotyy(k, 10*log10(pout_ratio_k_delta), k,
RL*peak_sscpt_k_delta);
xlabel('Value of k');
set(get(AX(1),'Ylabel'),'String','Zero-Point Power Ratio (dB)');
set(get(AX(2),'Ylabel'),'String','Susceptance Normalized to RL');
title('4-Way Power Combiner Design Curves');
grid on;
```

Appendix D

# Schematics, Bill-of-Materials, and PCB Artwork

## D.1. The Outphaser PCB

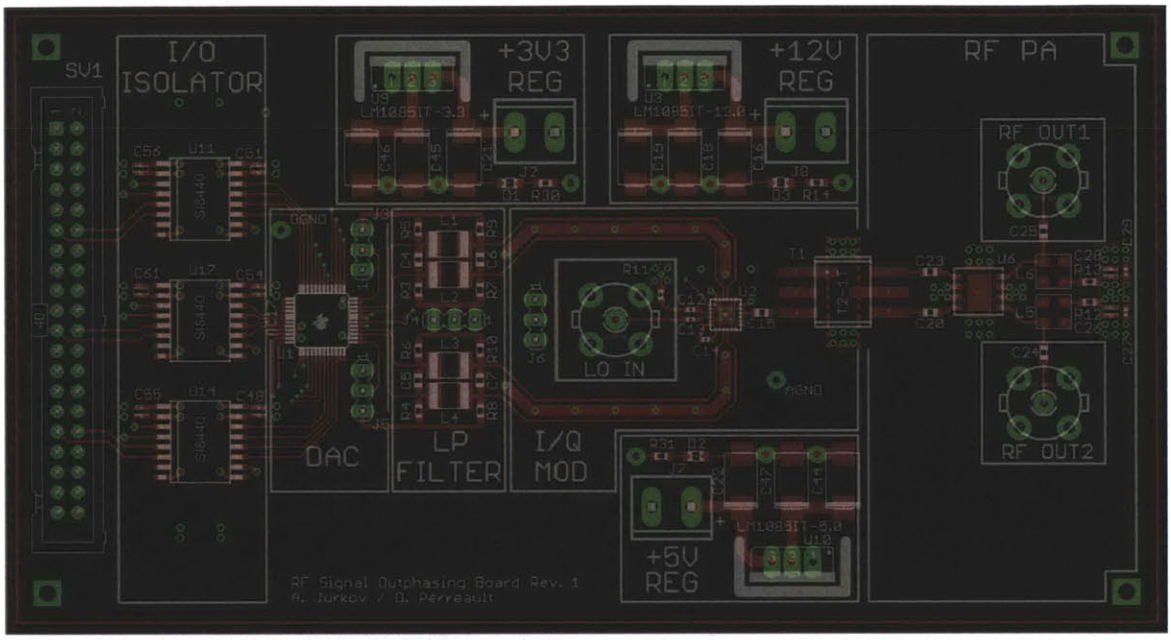



Fig. D-1: Outphaser PCB top layer copper/silkscreen

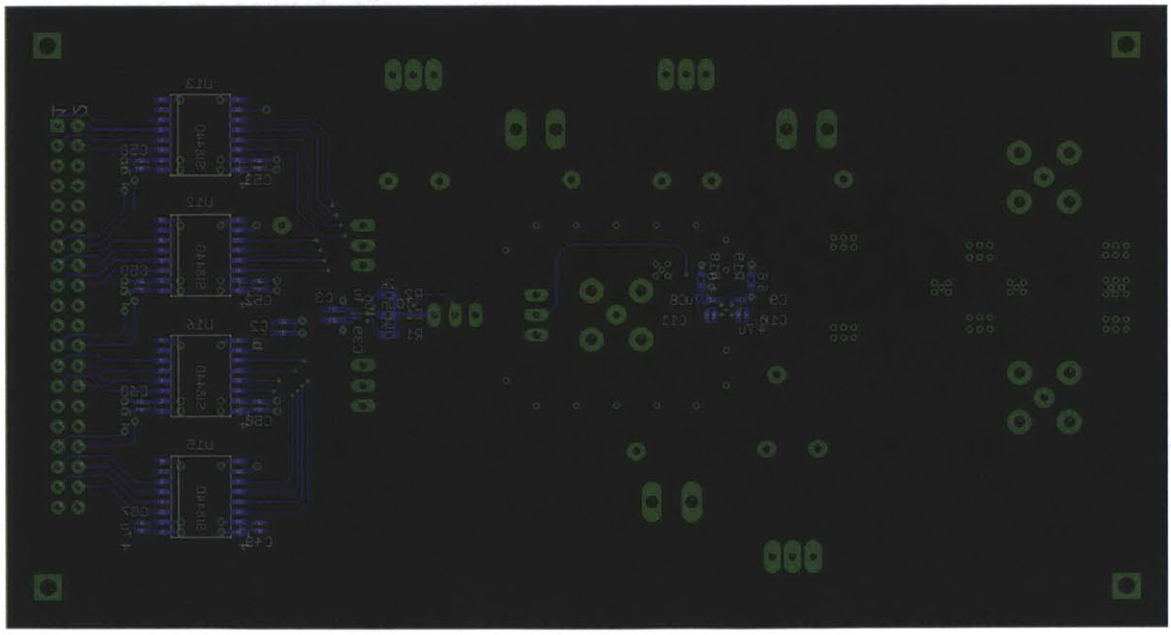


Fig. D-2: Outphaser PCB bottom layer copper/silkscreen

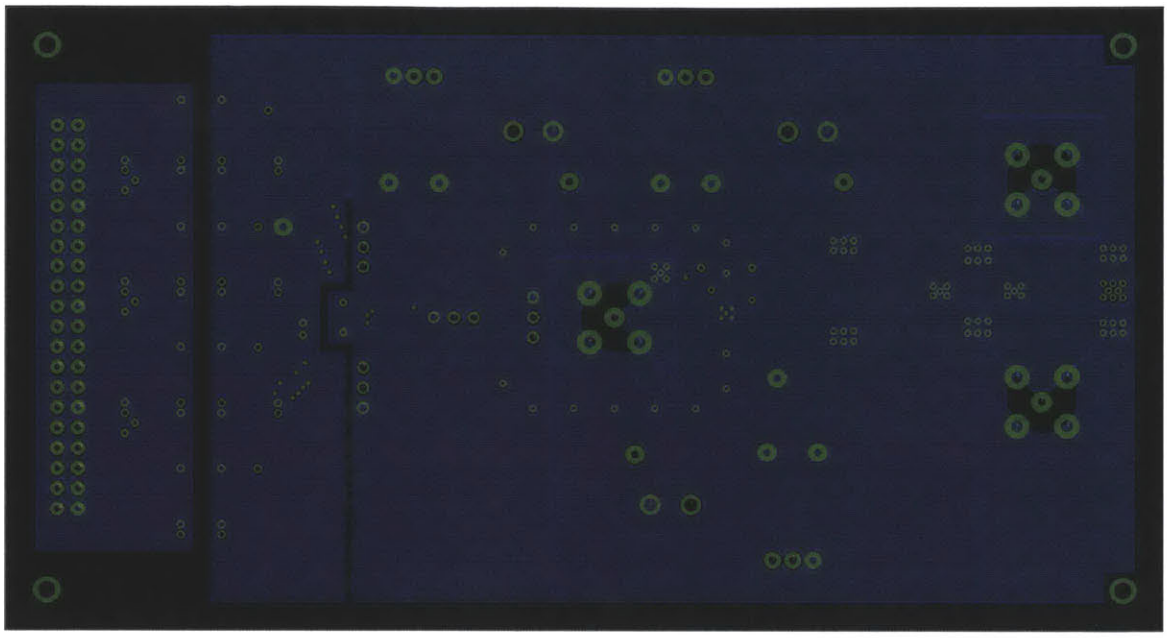


Fig. D-3: Outphaser PCB GND layer copper (2nd layer from the top)

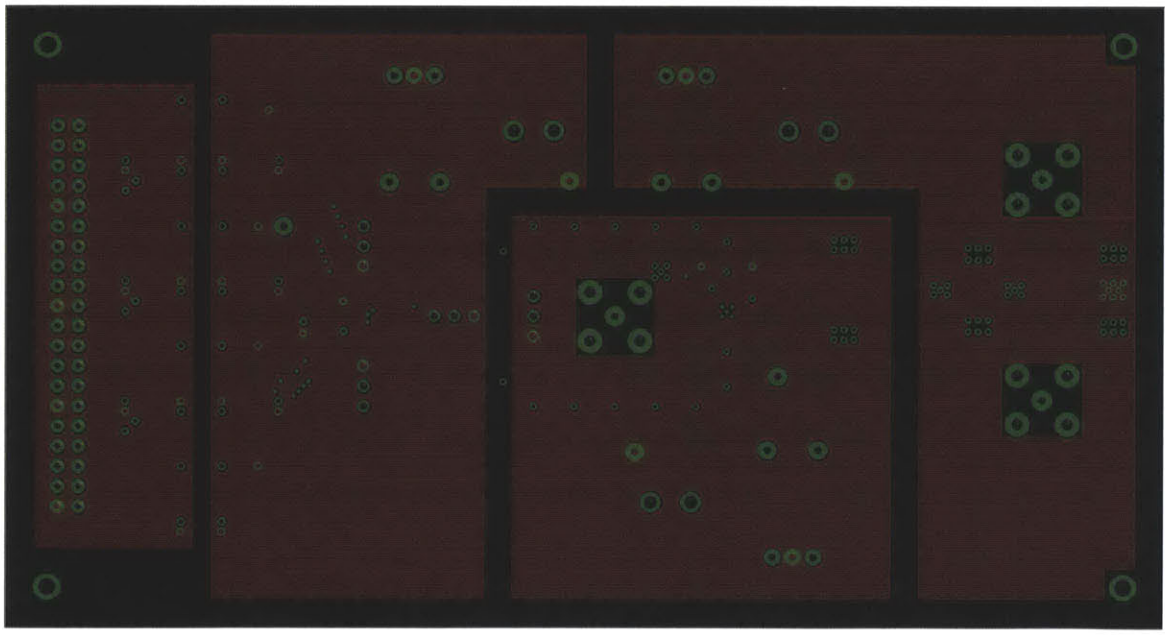


Fig. D-4: Outphaser PCB VDD layer copper (3rd layer from the top)

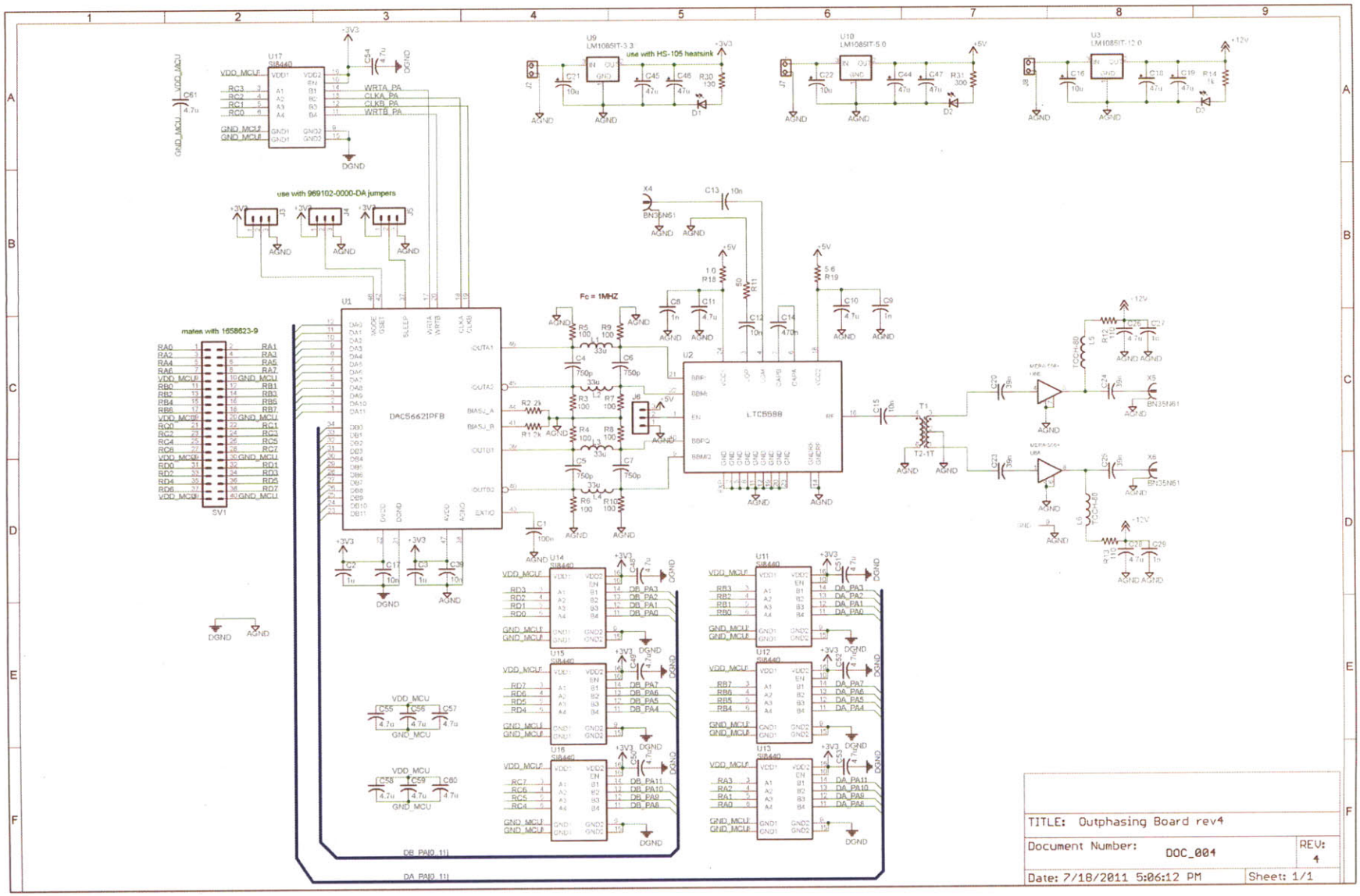

use with HS-105 heatsink
use with 969102-0000-DA jumpers
mates with 1658623-9
Fc = 1MHZ
DAC5662IPFB
LTC6588
TITLE: Outphasing Board rev4
Document Number: DOC_001
REV: 4
Date: 7/18/2011 5:06:12 PM
Sheet: 1/1

TABLE D1: OUTPHASER PCB BILL-OF-MATERIALS

| Parts | Value | Package | Description | Manufacturer | Manufacturer Part# | Qty |
|---|---|---|---|---|---|---|
| J2, J7, J8 | Header, Male Pins, Shrouded (2 Side) | Through Hole, 5.08MM Pitch | TERM BLOCK HDR 2POS VERT 5.08MM | TE Connectivity | 282825-2 | 3 |
| D1, D2, D3 | | 0805 (2012 Metric) | LED GRN S-TYPE GULL WING SMD | Panasonic - SSG | LNJ306G5TR02 | 3 |
| J3, J4, J5, J6 | Header, Unshrouded | Through Hole, 2.54MM Pitch | BERGSTIK II .100" SR STRAIGHT | FCI | 68000-203HLF | 4 |
| SV1 | Header, Shrouded | Through Hole, 2.54MM Pitch | CONN HEADER VERT 40POS .100 15AU | TE Connectivity | 5499922-9 | 1 |
| R18 | 1 | 0603 (1608 Metric) | RES 1.00 OHM 1/10W 1% 0603 SMD | Yageo | RC0603FR-071RL | 1 |
| R14 | 1k | 0603 (1608 Metric) | RES 1.0K OHM 1/10W 5% 0603 SMD | Yageo | RC0603JR-071KL | 1 |
| C8, C9, C27, C29 | 1n | 0402 (1005 Metric) | CAP CER 1000PF 50V 10% X7R 0402 | Murata Electronics North America | GRM155R71H102KA01D | 4 |
| C2, C3 | 1u | 1206 (3216 Metric) Wide (Long Side), 0612 (1632 Metric) | CAP CER 1.0UF 16V 10% X7R 0612 | TDK Corporation | C1632X7R1C105K | 2 |
| R1, R2 | 2k | 0603 (1608 Metric) | RES 2.0K OHM 1/10W .05% 0603 SMD | Susumu | RG1608N-202-W-T1 | 2 |

| | | | | | | |
|---|---|---|---|---|---|---|
| C10, C11, C26, C28, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61 | 4.7u | 0805 (2012 Metric) Wide (Long Side), 0508 (1220 Metric) | CAP CER 4.7UF 6.3V X6S 0508 | Taiyo Yuden | JWK212C6475KD-T | 18 |
| R19 | 5.6 | 0603 (1608 Metric) | RES 5.60 OHM 1/10W 1% 0603 SMD | Vishay/Dale | CRCW06035R60FKEA | 1 |
| C17, C39 | 10n | 0603 (1608 Metric) Wide (Long Side), 0306 (0816 Metric) | CAP CER .01UF 16V 10% X7R 0306 | TDK Corporation | C0816X7R1C103K | 2 |
| C12, C13 | 10n | 0402 (1005 Metric) | CAP .01UF 25V CERAMIC X7R 0402 | Kemet | C0402C103J3RACTU | 2 |
| C15 | 10n | 0603 (1608 Metric) | CAP CER 10000PF 50V X7R 5% 0603 | AVX Corporation | 06035C103JAT2A | 1 |
| C16, C21, C22 | 10u | 2917 (7343 Metric) | CAP TANT 10UF 35V 10% SMD | Vishay/Sprague | TR3D106K035C0250 | 3 |
| L1, L2, L3, L4 | 33u | 1008 (2520 Metric) | INDUCTOR POWER 33UH 1008 | TDK Corporation | NLV25T-330J-PF | 4 |
| C20, C23, C24, C25 | 39n | 0603 (1608 Metric) | CAP CER .039UF 10% 50V X7R 0603 | AVX Corporation | 06035C393KAT2A | 4 |

| | | | | | | |
|---|---|---|---|---|---|---|
| C18, C19, C44, C45, C46, C47 | 47u | 2917 (7343 Metric) | CAP TANT 47UF 20V 10% 2917 | AVX Corporation | TPSD476K020R0100 | 6 |
| R11 | 50 | 0603 (1608 Metric) | RES 50 OHM 125MW .1% 0603 SMD | Vishay/Thin Film | FC0603E50R0BTBS T1 | 1 |
| R3, R4, R5, R6, R7, R8, R9, R10 | 100 | 0603 (1608 Metric) | RES 100 OHM 1/10W 0.1% 0603 | Vishay/Dale | TNPW0603100RBEE A | 8 |
| C1 | 100n | 0603 (1608 Metric) | CAP CER .1UF 16V 10% X7R 0603 | Murata Electronics North America | GRM188R71C104KA 01D | 1 |
| R12, R13 | 220 | 0805 (2012 Metric) | RES 220 OHM 1/4W 1% 0805 SMD | Rohm Semiconductor | ESR10EZPF2200 | 4 |
| R30 | 130 | 0603 (1608 Metric) | RES 130 OHM 1/10W 5% 0603 SMD | Yageo | RC0603JR-07130RL | 1 |
| R31 | 300 | 0603 (1608 Metric) | RES 300 OHM 1/10W 5% 0603 SMD | Yageo | RC0603JR-07300RL | 1 |
| C14 | 470n | 0402 (1005 Metric) | CAP CER .47UF 10V X5R 0402 | Murata Electronics North America | GRM155R61A474KE 15D | 1 |
| C4, C5, C6, C7 | 750p | 0603 (1608 Metric) | CAP CER 750PF 50V 5% C0G 0603 | Murata Electronics North America | GRM1885C1H751JA 01D | 4 |
| X4, X5, X6 | BN35N 61 | Through Hole | CONN SOCKET BNC STR 50 OHM PCB | TE Connectivity | 5-1634503-1 | 3 |
| U1 | DAC56 62IPFB | 48-TQFP | IC DAC 12BIT 200MSPS DUAL 48TQFP | Texas Instruments | DAC5662IPFB | 1 |
| U9 | LM108 5IT-3.3 | TO-220-3 | IC REG POSITIVE 3A LDO TO220-3 | National Semiconductor | LM1085IT-3.3/NOPB | 1 |

| | | | | | | |
|---|---|---|---|---|---|---|
| U10 | LM1085IT-5.0 | TO-220-3 | IC REG POSITIVE 3A LDO TO220-3 | National Semiconductor | LM1085IT-5.0-ND | 1 |
| U3 | LM1085IT-12.0 | TO-220-3 | IC REG POSITIVE 3A LDO TO220-3 | National Semiconductor | LM1085IT-12/NOPB | 1 |
| U2 | LTC5598 | 24-WFQFN Exposed Pad | IC MODULATOR QUADRATURE 24-QFN | Linear Technology | LTC5598IUF#PBF | 1 |
| U6 | MERA-556+ | DL1020 | Amplifier, Monolithic, Dual Matched, RoHS | Mini-Circuits | MERA-556+ | 1 |
| U11, U12, U13, U14, U15, U16, U17 | SI8440 | 16-SOICW | IC ISOLATOR 4CH 5.5V 16-SOIC | Silicon Laboratories Inc | SI8440BB-D-IS | 7 |
| T1 | T2-1T | KK81 | Transformer, RF, RoHS5 | Mini-Circuits | T2-1T-KK81 | 1 |
| L5, L6 | TCCH-80 | GU1604 | RF Choke, RoHS | Mini-Circuits | TCCH-80+ | 2 |
| **Additional Components/Mounting Hardware** | | | | | | |
| N/A | N/A | N/A | CONN IDC SOCKET 40POS GOLD | TE Connectivity | 1658623-9 | 1 |
| N/A | N/A | N/A | HEAT SINK TO-220 .250" COMPACT | Aavid Thermalloy | 577002B00000G | 3 |
| N/A | N/A | N/A | TERM BLOCK PLUG 2POS VERT 5.08MM | TE Connectivity | 284041-2 | 3 |
| N/A | N/A | N/A | SHUNT JUMPER .1" BLACK GOLD | 3M | 969102-0000-DA | 4 |
| N/A | N/A | N/A | CONN IDC SOCKET 10POS 15 GOLD | TE Connectivity | 1658620-1 | 4 |
| N/A | N/A | N/A | STDOFF HEX FLA-RET 4-40 1.000"L | Keystone Electronics | 8440G | 4 |

| | | | | | | |
|---|---|---|---|---|---|---|
| N/A | N/A | N/A | SCREW MACH PHIL 4-40X1/2 NYLON | B&F Fastener Supply | NY PMS 440 0050 PH | 4 |
| N/A | N/A | N/A | STANDOFF HEX 2-56THR .375"L ALUM | Keystone Electronics | 1797D | 4 |
| N/A | N/A | N/A | SCREW MACHINE PHILLIPS 2-56X1/4 | B&F Fastener Supply | PMS 256 0025 PH | 4 |

## D.2. Four-Way Combiner PCB

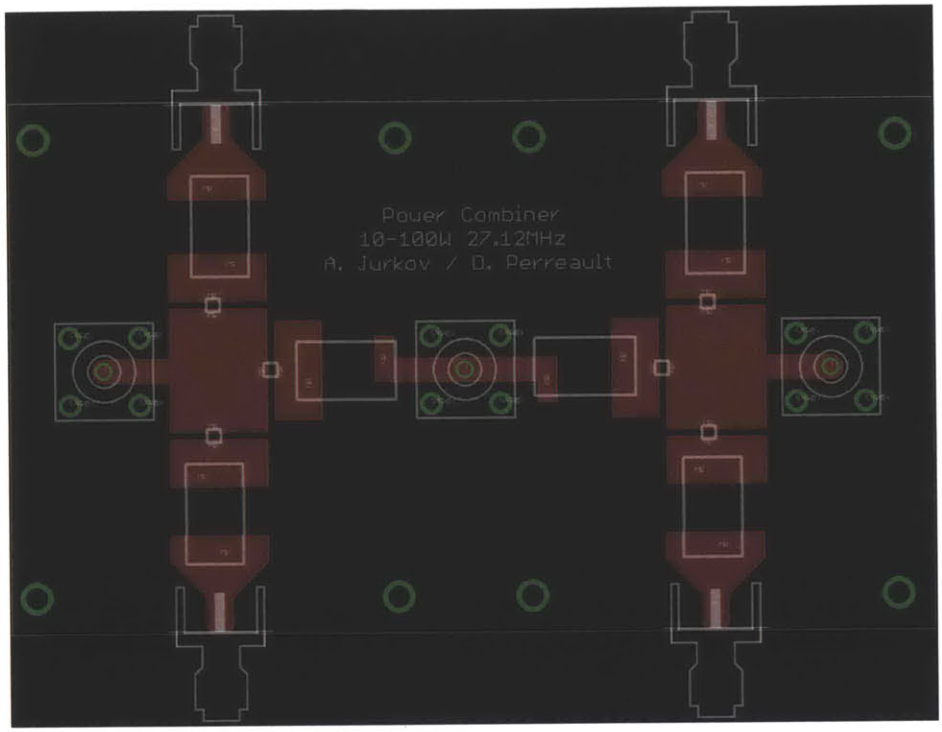



Fig. D-5: Four-way power combiner PCB (top layer copper/silkscreen)

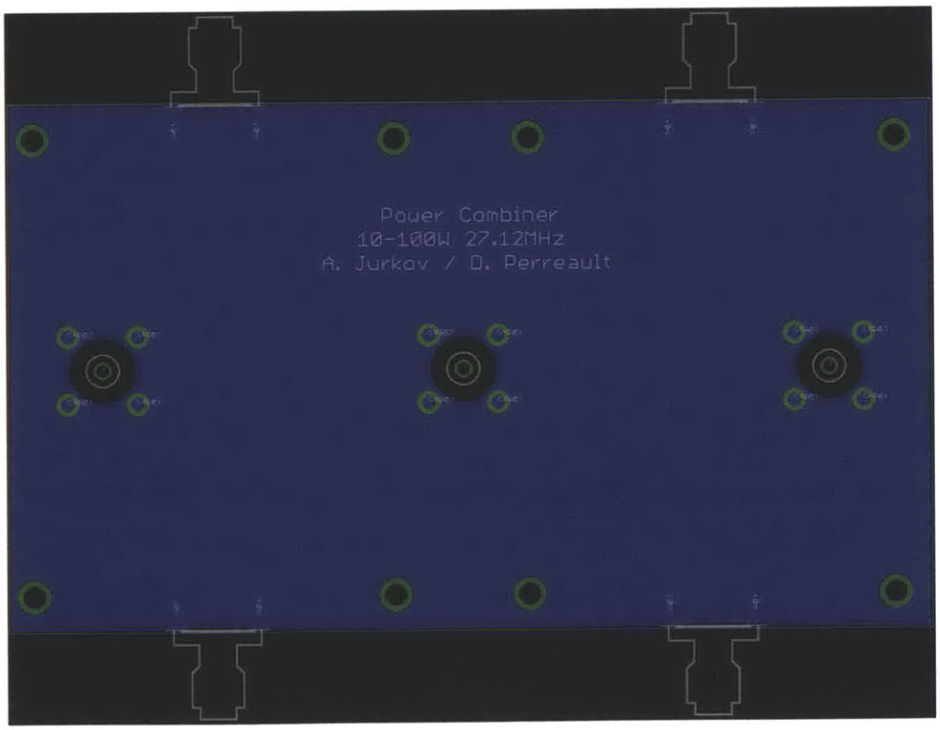
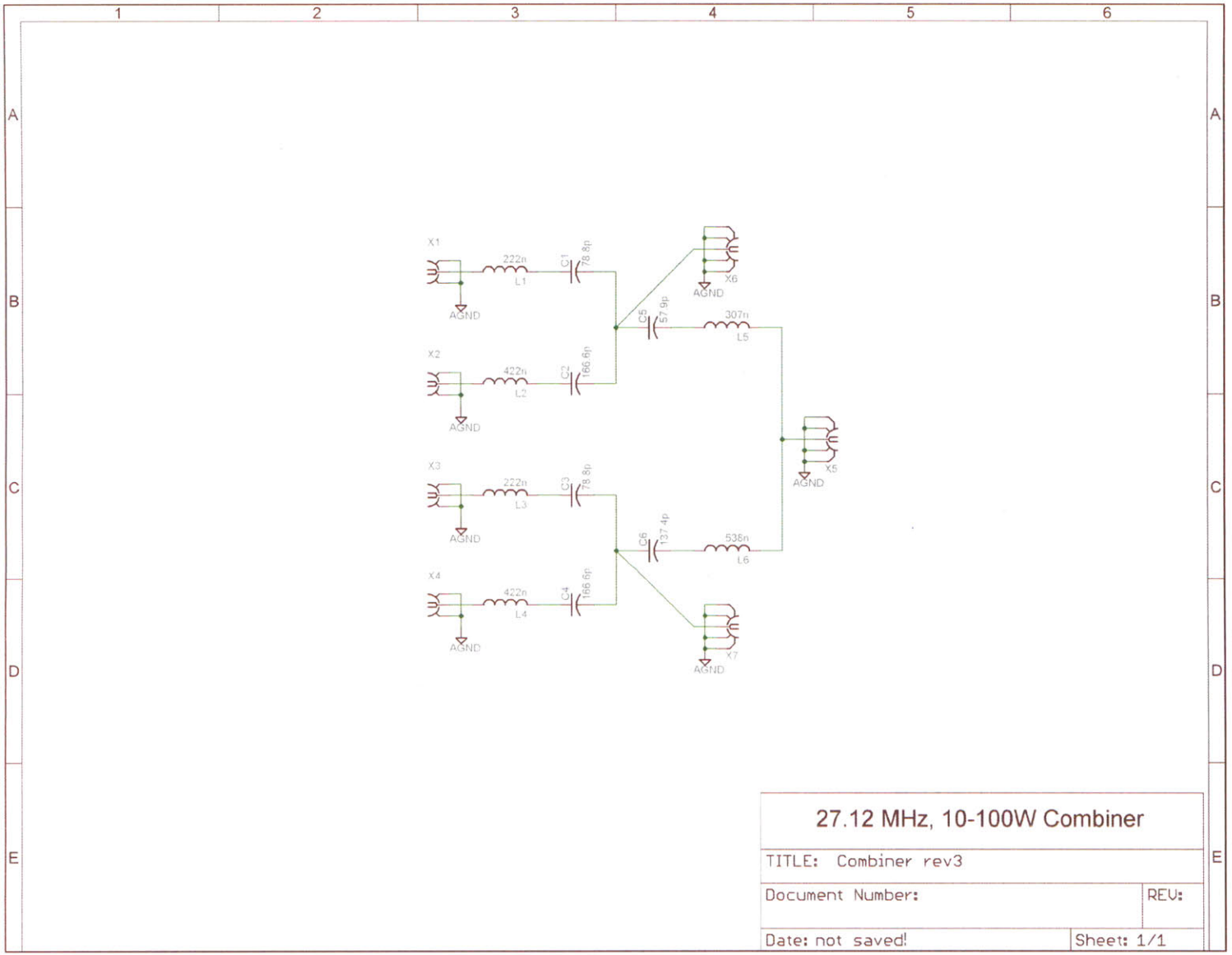



Fig. D-6: Four-way power combiner PCB (bottom layer copper/silkscreen)


1
2
3
4
5
6
A
B
C
D
E
X1
222n
L1
C1
78.8p
AGND
X2
422n
L2
C2
166.6p
AGND
X3
222n
L3
C3
78.8p
AGND
X4
422n
L4
C4
166.6p
AGND
C5
57.9p
C6
137.4p
X6
AGND
307n
L5
X5
AGND
538n
L6
X7
AGND
27.12 MHz, 10-100W Combiner
TITLE: Combiner rev3
Document Number:
REV:
Date: not saved!
Sheet: 1/1

## D.3. Class-E Power Amplifier PCB

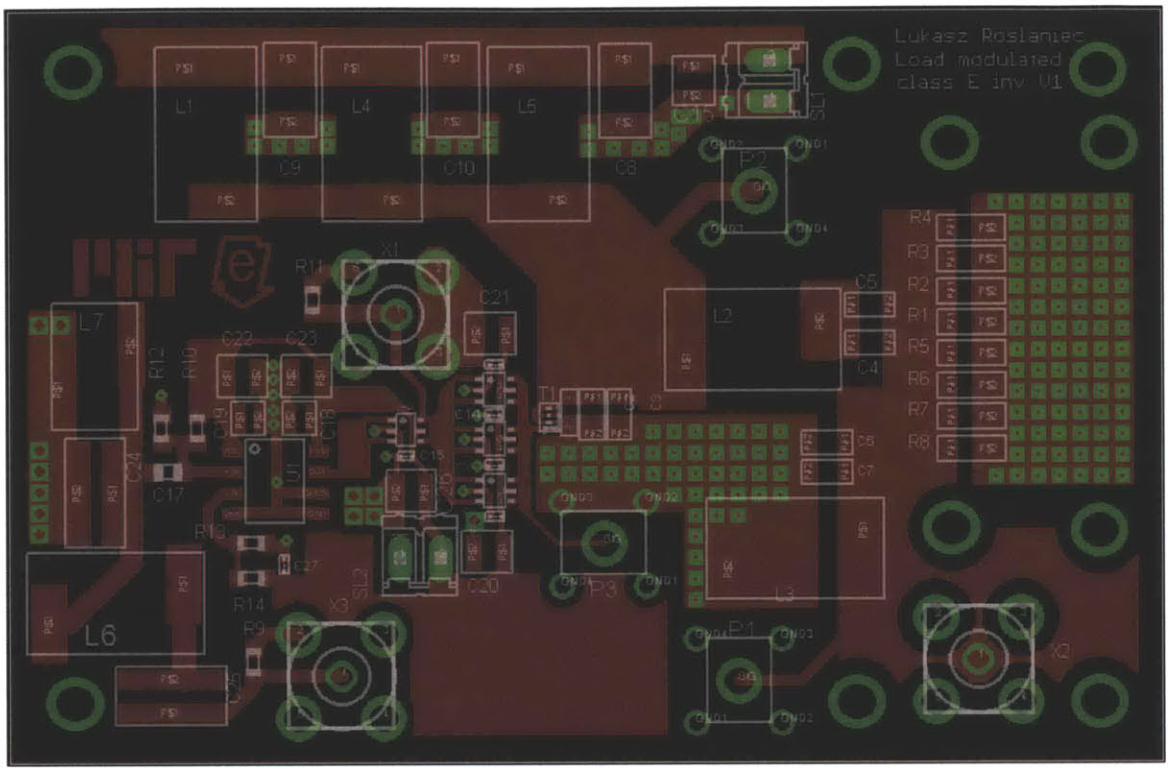



Fig. D-7: Class-E PA PCB (top layer copper/silkscreen)

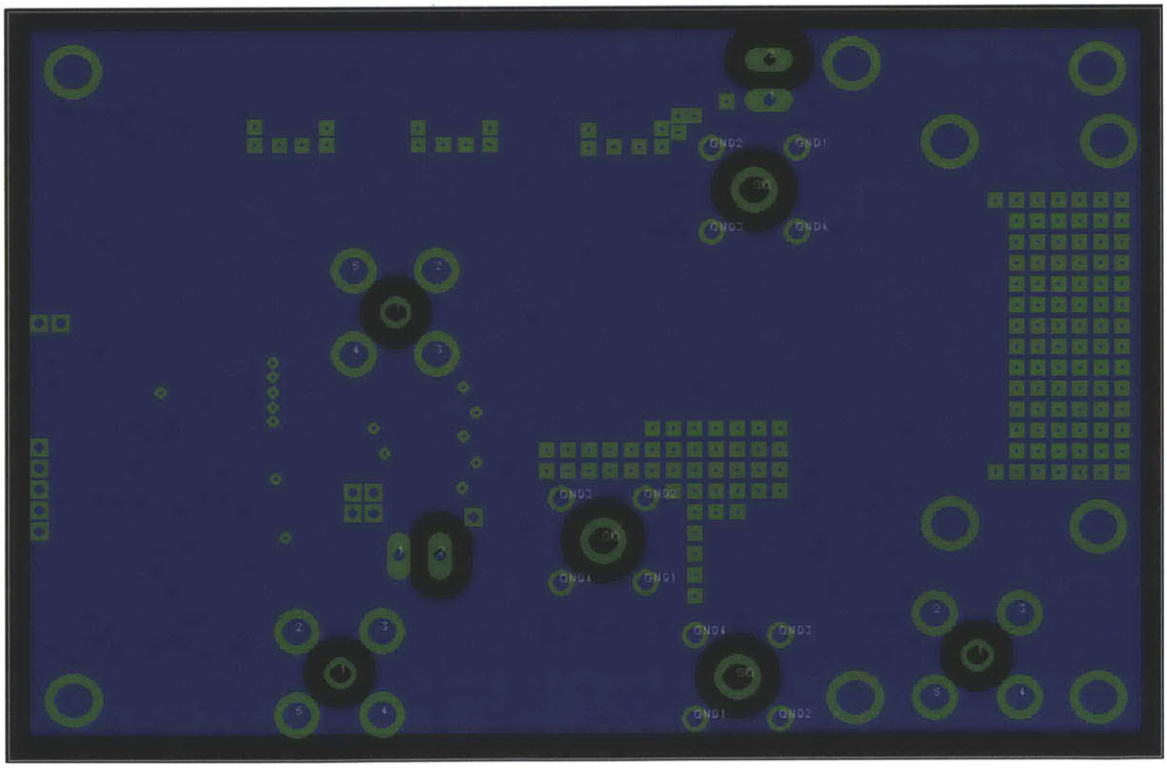


Fig. D-8: Class-E PCB (bottom layer copper/silkscreen)

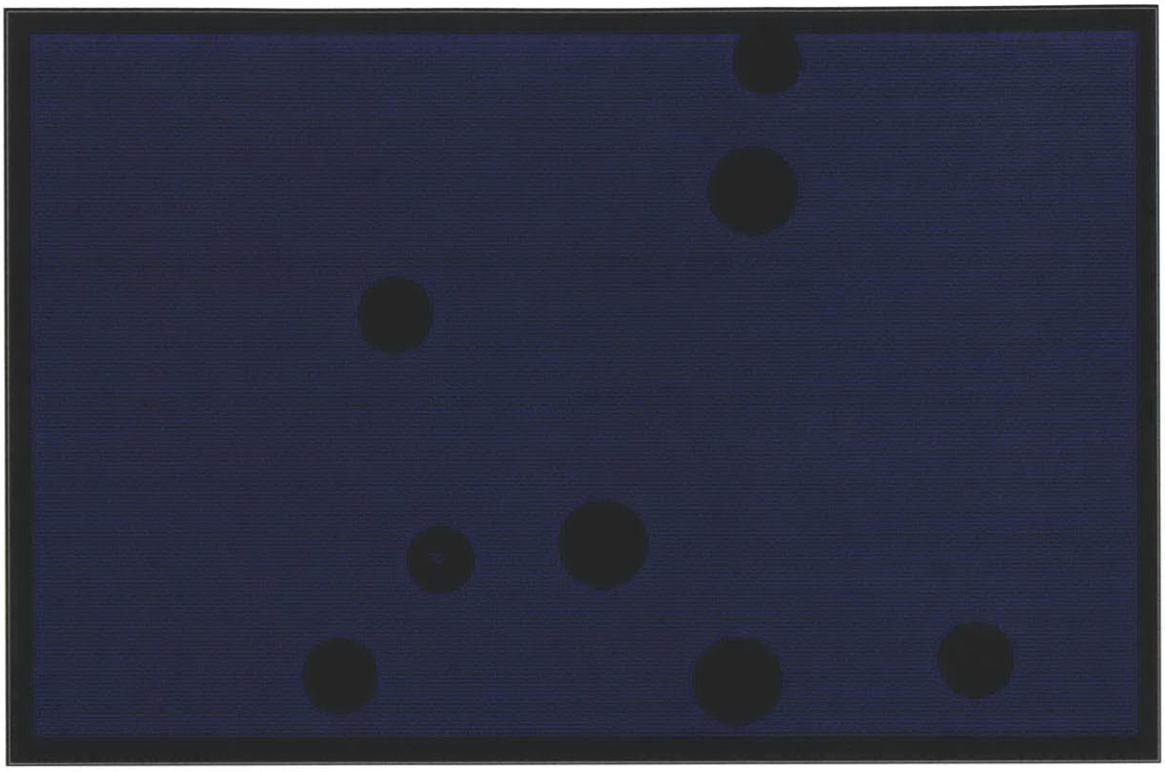


Fig. D-9: Class-E PCB GND layer (1st inner layer from top)

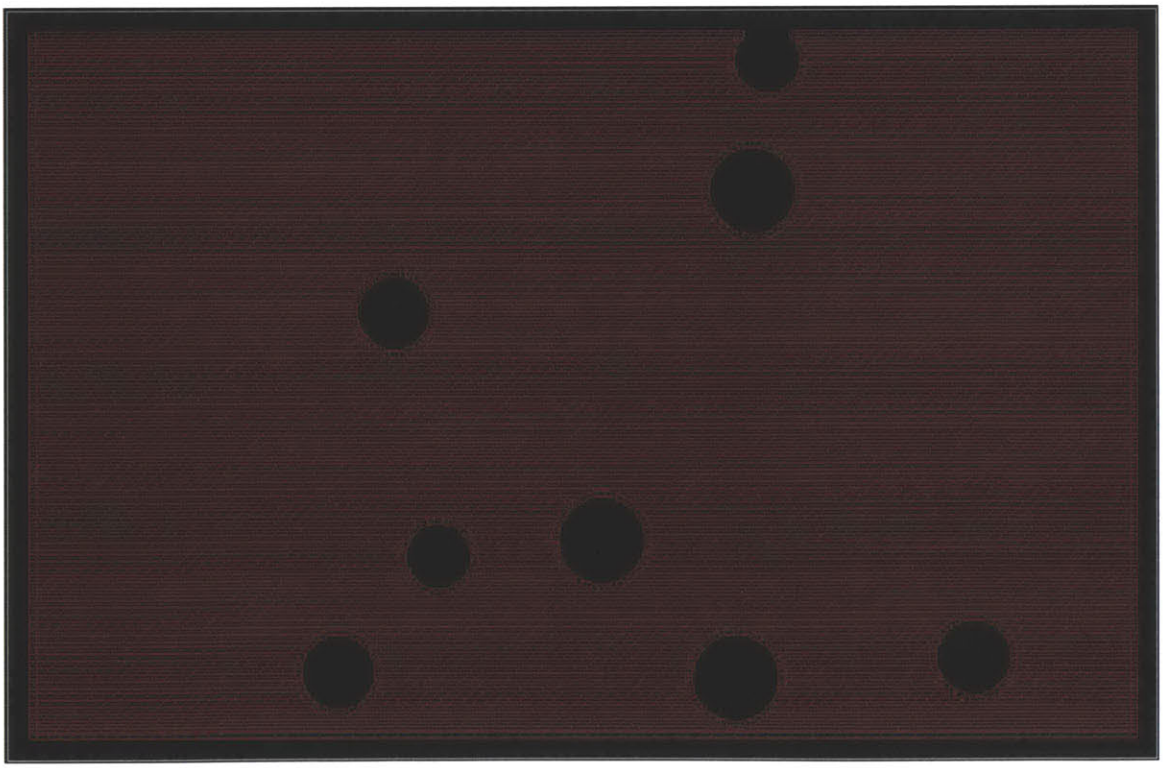
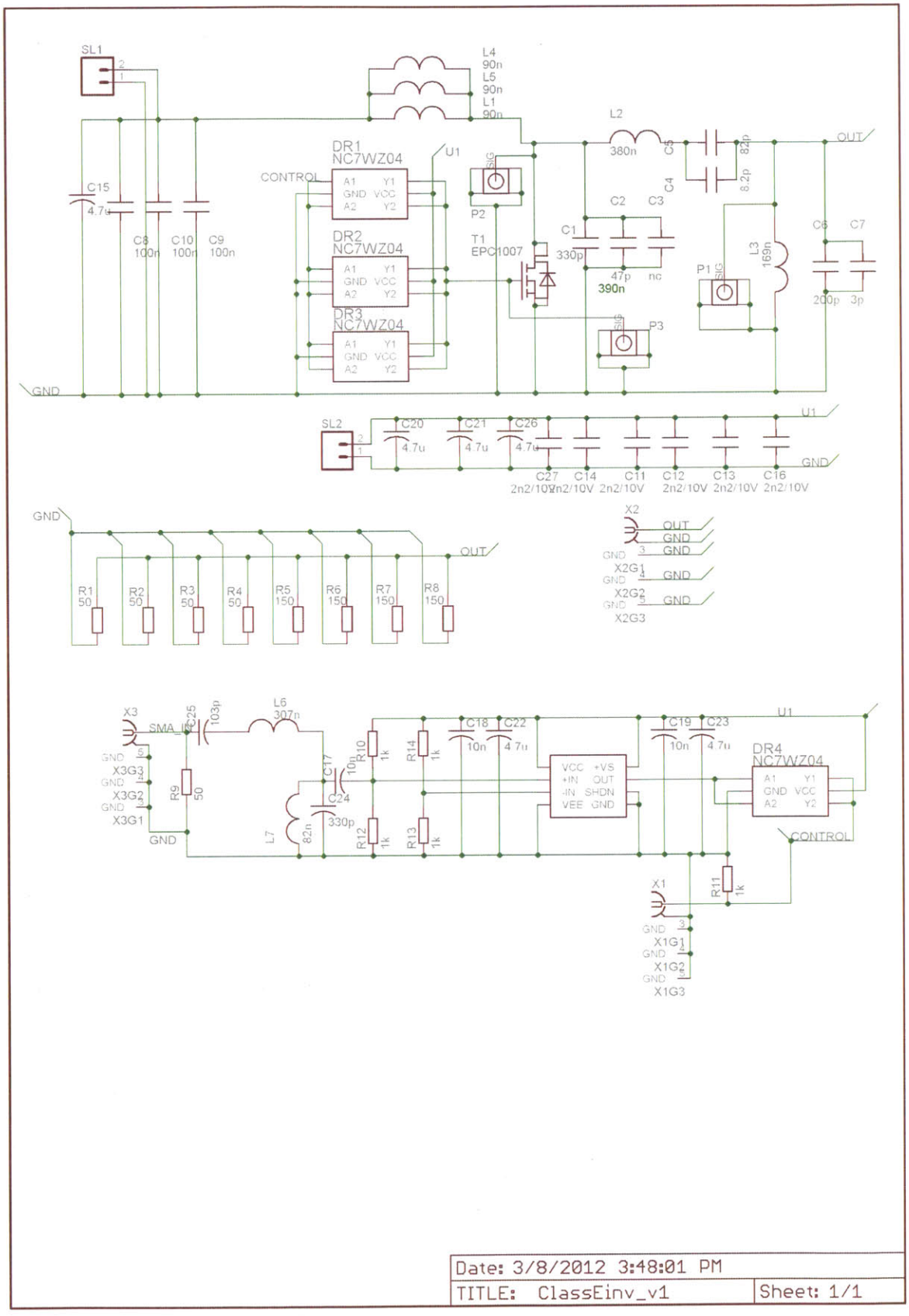


Fig. D-10: Class-E PCB VDD layer (2nd inner layer from top)




| | |
|---|---|
| Date: 3/8/2012 3:48:01 PM | |
| TITLE: ClassEinv_v1 | Sheet: 1/1 |

## Appendix E

# PIC32MX460 Microcontroller Firmware

phase_shifter_v2.c

```
/*
 * Name: phase_shifter_v2.c
 * Description: Manually set the outphasing angle of each of the four outphaser
 *          PCBs (A, B, C, D). The outphasing angle of each outphaser is
 *          set via a pair of 12-bit integers which represnt the voltage on
 *          the respective I and Q modulator channels (set through a DAC).
 *          RG15/RG3 - increment/decrement A outphasing angle
 *          RG14/RG2 - increment/decrement B outphasing angle
 *          RG13/RG1 - increment/decrement C outphasing angle
 *          RG12/RG0 - increment/decrement D outphasing angle
 * Last Update: Nov. 23, 2011
 */

#define SIZE1 8
#include <built_in.h>

// DAC codes for outphaser A
unsigned int AI_value[SIZE1] = {3139, 3139, 3139, 3139, 3139, 3139, 3139, 3139};
unsigned int AQ_value[SIZE1] = {2048, 2048, 2048, 2048, 2048, 2048, 2048, 2048};

// DAC codes for outphaser B
unsigned int BI_value[SIZE1] = {1016, 1002, 1083, 1296, 1668, 2105, 2450, 2634};
unsigned int BQ_value[SIZE1] = {2428, 1710, 1519, 1242, 1010,  944, 1019, 1113};

// DAC codes for outphaser C
unsigned int CI_value[SIZE1] = {985 , 1538 , 1763 , 1960 , 2033 , 1960 , 1759 , 1531};
unsigned int CQ_value[SIZE1] = {2359 , 1056 ,  968 ,  934 ,  930 ,  934 ,  969 , 1060};

// DAC codes for outphaser D
unsigned int DI_value[SIZE1] = {1316 , 3097 , 3127 , 2925 , 2540 , 2188 , 2039 , 2076};
unsigned int DQ_value[SIZE1] = {1237 , 1755 , 2194 , 2695 , 3022 , 3131 , 3140 , 3140};

unsigned long index1 = 0;  // index to I_value and Q_value
unsigned int data_i = 2048;
unsigned int data_q = 2048;
unsigned int num = 1; // active channel number

double m_ia = 2.1830;
double m_qa = 2.2072;
double n_ia = 2047.4;
double n_qa = 2047.7;

double m_ib = 2.1959;
double m_qb = 2.2115;
double n_ib = 2047.5;
double n_qb = 2047.8;
```

```
double m_ic = 2.2135;
double m_qc = 2.2339;
double n_ic = 2047.4;
double n_qc = 2047.3;

double m_id = 2.1780;
double m_qd = 2.1867;
double n_id = 2047.8;
double n_qd = 2047.1;

void set_phase_a(void);  // set the outphasing angle of outphaser A
void set_phase_b(void);  // set the outphasing angle of outphaser B
void set_phase_c(void);  // set the outphasing angle of outphaser C
void set_phase_d(void);  // set the outphasing angle of outphaser D

void main() {
  double CODE_I;
  double CODE_Q;

  DDPCON.JTAGEN=0;
  AD1PCFG = 0xFFFFFFFF;              // Configure AN pins as digital I/O

  TRISA = 0x0000C000;
  PORTA = 0;
  TRISB = 0;
  PORTB = 0;
  TRISC = 0xFF;
  TRISD = 0;
  PORTD = 0;
  TRISE = 0;
  PORTE = 0;
  TRISF = 0;
  PORTF = 0;
  TRISG = 0;
  PORTG = 0;

  // Initialize outphasers
  set_phase_a();
  set_phase_b();
  set_phase_c();
  set_phase_d();

  while(1){
   if(PORTA.B15){
    index1+=1;
    if(index1 > SIZE1-1) index1 = SIZE1-1;
    set_phase_a();
    set_phase_b();
    set_phase_c();
    set_phase_d();
    while(PORTA.B15){}
    Delay_ms(20);
   }
   if(PORTA.B14){
    index1-=1;
    if(index1 > SIZE1-1) index1 = 0;
```

```
 set_phase_a();
 set_phase_b();
 set_phase_c();
 set_phase_d();
 while(PORTA.B14){}
 Delay_ms(20);
 }
 if(PORTC.B2){
 num+=1;
 if(num > 4) num=4;
 while(PORTC.B2){}
 Delay_ms(20);
 }
 if(PORTC.B1){
 num-=1;
 if(num < 1) num = 1;
 while(PORTC.B1){}
 Delay_ms(20);
 }
 if(PORTC.B4){
 if(num==1){
  AI_value[index1]+=10;
  if(AI_value[index1]>4095) AI_value[index1]=4095;
  CODE_I = (double) AI_value[index1];
  CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ia)/m_ia),2))*m_qa+n_qa;
  AQ_value[index1] = (unsigned int) CODE_Q;
 }
 if(num==2){
  BI_value[index1]+=10;
  if(BI_value[index1]>4095) BI_value[index1]=4095;
  CODE_I = (double) BI_value[index1];
  CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ib)/m_ib),2))*m_qb+n_qb;
  BQ_value[index1] = (unsigned int) CODE_Q;
 }
 if(num==3){
  CI_value[index1]+=10;
  if(CI_value[index1]>4095) CI_value[index1]=4095;
  CODE_I = (double) CI_value[index1];
  CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ic)/m_ic),2))*m_qc+n_qc;
  CQ_value[index1] = (unsigned int) CODE_Q;
 }
 if(num==4){
  DI_value[index1]+=10;
  if(DI_value[index1]>4095) DI_value[index1]=4095;
  CODE_I = (double) DI_value[index1];
  CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_id)/m_id),2))*m_qd+n_qd;
  DQ_value[index1] = (unsigned int) CODE_Q;
 }
 set_phase_a();
 set_phase_b();
 set_phase_c();
 set_phase_d();
 //while(PORTC.B4){}
 Delay_ms(100);
 }
 if(PORTC.B3){
```

```
    if(num==1){
     AI_value[index1]-=10;
     if(AI_value[index1]>4095) AI_value[index1]=0;
     CODE_I = (double) AI_value[index1];
     CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ia)/m_ia),2))*m_qa+n_qa;
     AQ_value[index1] = (unsigned int) CODE_Q;
    }
    if(num==2){
     BI_value[index1]-=10;
     if(BI_value[index1]>4095) BI_value[index1]=0;
     CODE_I = (double) BI_value[index1];
     CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ib)/m_ib),2))*m_qb+n_qb;
     BQ_value[index1] = (unsigned int) CODE_Q;
    }
    if(num==3){
     CI_value[index1]-=10;
     if(CI_value[index1]>4095) CI_value[index1]=0;
     CODE_I = (double) CI_value[index1];
     CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_ic)/m_ic),2))*m_qc+n_qc;
     CQ_value[index1] = (unsigned int) CODE_Q;
    }
    if(num==4){
     DI_value[index1]-=10;
     if(DI_value[index1]>4095) DI_value[index1]=0;
     CODE_I = (double) DI_value[index1];
     CODE_Q = sqrt((double) 250000 - pow(((CODE_I-n_id)/m_id),2))*m_qd+n_qd;
     DQ_value[index1] = (unsigned int) CODE_Q;
    }
    set_phase_a();
    set_phase_b();
    set_phase_c();
    set_phase_d();
    //while(PORTC.B3){}
    Delay_ms(100);
   }

  }

  return;
}

void set_phase_a(void){
 data_i = AI_value[index1];
 data_q = AQ_value[index1];

/*****************************************************/
 PORTA = Hi(data_i);
 PORTB = Lo(data_i);
 PORTASET = 0x0030; // RESTEIQ(RA5) = 1, SELECTIQ(RA4) = 1
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0

 PORTA = Hi(data_q); // Also clears RA5 and RA4
 PORTB = Lo(data_q);
 PORTACLR = 0x0030; // RESTEIQ(RA5) = 0, SELECTIQ(RA4) = 0 (for redundancy)
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
```

```
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0
/*****************************************************/
 PORTA = Hi(data_i);
 PORTB = Lo(data_i);
 PORTASET = 0x0030; // RESTEIQ(RA5) = 1, SELECTIQ(RA4) = 1
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0

 PORTA = Hi(data_q); // Also clears RA5 and RA4
 PORTB = Lo(data_q);
 PORTACLR = 0x0030; // RESTEIQ(RA5) = 0, SELECTIQ(RA4) = 0 (for redundancy)
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0
/*****************************************************/
 PORTA = Hi(data_i);
 PORTB = Lo(data_i);
 PORTASET = 0x0030; // RESTEIQ(RA5) = 1, SELECTIQ(RA4) = 1
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0

 PORTA = Hi(data_q); // Also clears RA5 and RA4
 PORTB = Lo(data_q);
 PORTACLR = 0x0030; // RESTEIQ(RA5) = 0, SELECTIQ(RA4) = 0 (for redundancy)
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0
/*****************************************************/
 PORTA = Hi(data_i);
 PORTB = Lo(data_i);
 PORTASET = 0x0030; // RESTEIQ(RA5) = 1, SELECTIQ(RA4) = 1
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0

 PORTA = Hi(data_q); // Also clears RA5 and RA4
 PORTB = Lo(data_q);
 PORTACLR = 0x0030; // RESTEIQ(RA5) = 0, SELECTIQ(RA4) = 0 (for redundancy)
 PORTASET = 0x00C0; // WRTIQ(RA7) = 1, CLKIQ(RA6) = 1
 PORTACLR = 0x00C0; // WRTIQ(RA7) = 0, CLKIQ(RA6) = 0
/*****************************************************/

 return;
}

void set_phase_b(void){
 data_i = BI_value[index1];
 data_q = BQ_value[index1];

/*****************************************************/
 PORTB = Hi(data_i) << 8;
 PORTD = Lo(data_i);
 PORTBSET = 0x3000; // RESTEIQ(RB13) = 1, SELECTIQ(RB132) = 1
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0

 PORTB = Hi(data_q) << 8; // Also clears RB12 and RB13
 PORTD = Lo(data_q);
 PORTBCLR = 0x3000; // RESTEIQ(RB13) = 0, SELECTIQ(RB12) = 0 (redundant)
```

```
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0
/*****************************************************/
 PORTB = Hi(data_i) << 8;
 PORTD = Lo(data_i);
 PORTBSET = 0x3000; // RESTEIQ(RB13) = 1, SELECTIQ(RB132) = 1
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0

 PORTB = Hi(data_q) << 8; // Also clears RB12 and RB13
 PORTD = Lo(data_q);
 PORTBCLR = 0x3000; // RESTEIQ(RB13) = 0, SELECTIQ(RB12) = 0 (redundant)
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0
/*****************************************************/
 PORTB = Hi(data_i) << 8;
 PORTD = Lo(data_i);
 PORTBSET = 0x3000; // RESTEIQ(RB13) = 1, SELECTIQ(RB132) = 1
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0

 PORTB = Hi(data_q) << 8; // Also clears RB12 and RB13
 PORTD = Lo(data_q);
 PORTBCLR = 0x3000; // RESTEIQ(RB13) = 0, SELECTIQ(RB12) = 0 (redundant)
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0
/*****************************************************/
 PORTB = Hi(data_i) << 8;
 PORTD = Lo(data_i);
 PORTBSET = 0x3000; // RESTEIQ(RB13) = 1, SELECTIQ(RB132) = 1
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0

 PORTB = Hi(data_q) << 8; // Also clears RB12 and RB13
 PORTD = Lo(data_q);
 PORTBCLR = 0x3000; // RESTEIQ(RB13) = 0, SELECTIQ(RB12) = 0 (redundant)
 PORTBSET = 0xC000; // WRTIQ(RB15) = 1, CLKIQ(RB14) = 1
 PORTBCLR = 0xC000; // WRTIQ(RB15) = 0, CLKIQ(RB14) = 0
/*****************************************************/
 return;
}

void set_phase_c(void){
 data_i = CI_value[index1];
 data_q = CQ_value[index1];

/*****************************************************/
 PORTD = Hi(data_i) << 8;
 PORTE = Lo(data_i);
 PORTDSET = 0x3000; // RESTEIQ(RD13) = 1, SELECTIQ(RD12) = 1
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0

 PORTD = Hi(data_q) << 8; // Also clears RD12 and RD13
 PORTE = Lo(data_q);
 PORTDCLR = 0x3000; // RESTEIQ(RD13) = 0, SELECTIQ(RD13) = 0 (redundant)
```

```
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0
/*****************************************************/
 PORTD = Hi(data_i) << 8;
 PORTE = Lo(data_i);
 PORTDSET = 0x3000; // RESTEIQ(RD13) = 1, SELECTIQ(RD12) = 1
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0

 PORTD = Hi(data_q) << 8; // Also clears RD12 and RD13
 PORTE = Lo(data_q);
 PORTDCLR = 0x3000; // RESTEIQ(RD13) = 0, SELECTIQ(RD13) = 0 (redundant)
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0
/*****************************************************/
 PORTD = Hi(data_i) << 8;
 PORTE = Lo(data_i);
 PORTDSET = 0x3000; // RESTEIQ(RD13) = 1, SELECTIQ(RD12) = 1
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0

 PORTD = Hi(data_q) << 8; // Also clears RD12 and RD13
 PORTE = Lo(data_q);
 PORTDCLR = 0x3000; // RESTEIQ(RD13) = 0, SELECTIQ(RD13) = 0 (redundant)
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0
/*****************************************************/
 PORTD = Hi(data_i) << 8;
 PORTE = Lo(data_i);
 PORTDSET = 0x3000; // RESTEIQ(RD13) = 1, SELECTIQ(RD12) = 1
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0

 PORTD = Hi(data_q) << 8; // Also clears RD12 and RD13
 PORTE = Lo(data_q);
 PORTDCLR = 0x3000; // RESTEIQ(RD13) = 0, SELECTIQ(RD13) = 0 (redundant)
 PORTDSET = 0xC000; // WRTIQ(RD15) = 1, CLKIQ(RD14) = 1
 PORTDCLR = 0xC000; // WRTIQ(RD15) = 0, CLKIQ(RD14) = 0
/*****************************************************/
 return;
}

void set_phase_d(void){
 unsigned long tmp1;
 unsigned long tmp2;
 data_i = DI_value[index1];
 data_q = DQ_value[index1];

/*****************************************************/
 tmp1 = Lo(data_i)&0x0F;
 tmp1 = tmp1 << 6;
 tmp2 = Lo(data_i)&0xF0;
 tmp2 = tmp2 << 8;
 PORTF = Hi(data_i);
 PORTG = tmp1 | tmp2;
 PORTFSET = 0x1100; // SELECTIQ(RF8) = 1, RESETIQ(RF12) = 1
```

```
PORTESET = 0x0200; // WRTIQ(RE9) = 1
PORTFSET = 0x2000; // CLKIQ(RF13)= 1
PORTECLR = 0x0200; // WRTIQ(RE9) = 0
PORTFCLR = 0x2000; // CLKIQ(RF13)= 0

tmp1 = Lo(data_q)&0x0F;
tmp1 = tmp1 << 6;
tmp2 = Lo(data_q)&0xF0;
tmp2 = tmp2 << 8;
PORTF = Hi(data_q); //Also clears RF8 and RF12
PORTG = tmp1 | tmp2;
PORTFCLR = 0x1100; // SELECTIQ(RF8) = 0, RESETIQ(RF12) = 0  (redundant)
PORTESET = 0x0200; // WRTIQ(RE9) = 1
PORTFSET = 0x2000; // CLKIQ(RF13)= 1
PORTECLR = 0x0200; // WRTIQ(RE9) = 0
PORTFCLR = 0x2000; // CLKIQ(RF13)= 0
/*****************************************************/
tmp1 = Lo(data_i)&0x0F;
tmp1 = tmp1 << 6;
tmp2 = Lo(data_i)&0xF0;
tmp2 = tmp2 << 8;
PORTF = Hi(data_i);
PORTG = tmp1 | tmp2;
PORTFSET = 0x1100; // SELECTIQ(RF8) = 1, RESETIQ(RF12) = 1
PORTESET = 0x0200; // WRTIQ(RE9) = 1
PORTFSET = 0x2000; // CLKIQ(RF13)= 1
PORTECLR = 0x0200; // WRTIQ(RE9) = 0
PORTFCLR = 0x2000; // CLKIQ(RF13)= 0

tmp1 = Lo(data_q)&0x0F;
tmp1 = tmp1 << 6;
tmp2 = Lo(data_q)&0xF0;
tmp2 = tmp2 << 8;
PORTF = Hi(data_q); //Also clears RF8 and RF12
PORTG = tmp1 | tmp2;
PORTFCLR = 0x1100; // SELECTIQ(RF8) = 0, RESETIQ(RF12) = 0  (redundant)
PORTESET = 0x0200; // WRTIQ(RE9) = 1
PORTFSET = 0x2000; // CLKIQ(RF13)= 1
PORTECLR = 0x0200; // WRTIQ(RE9) = 0
PORTFCLR = 0x2000; // CLKIQ(RF13)= 0
/*****************************************************/
tmp1 = Lo(data_i)&0x0F;
tmp1 = tmp1 << 6;
tmp2 = Lo(data_i)&0xF0;
tmp2 = tmp2 << 8;
PORTF = Hi(data_i);
PORTG = tmp1 | tmp2;
PORTFSET = 0x1100; // SELECTIQ(RF8) = 1, RESETIQ(RF12) = 1
PORTESET = 0x0200; // WRTIQ(RE9) = 1
PORTFSET = 0x2000; // CLKIQ(RF13)= 1
PORTECLR = 0x0200; // WRTIQ(RE9) = 0
PORTFCLR = 0x2000; // CLKIQ(RF13)= 0

tmp1 = Lo(data_q)&0x0F;
tmp1 = tmp1 << 6;
tmp2 = Lo(data_q)&0xF0;
```

```
    tmp2 = tmp2 << 8;
    PORTF = Hi(data_q); //Also clears RF8 and RF12
    PORTG = tmp1 | tmp2;
    PORTFCLR = 0x1100; // SELECTIQ(RF8) = 0, RESETIQ(RF12) = 0  (redundant)
    PORTESET = 0x0200; // WRTIQ(RE9) = 1
    PORTFSET = 0x2000; // CLKIQ(RF13)= 1
    PORTECLR = 0x0200; // WRTIQ(RE9) = 0
    PORTFCLR = 0x2000; // CLKIQ(RF13)= 0
   /*****************************************************/
    tmp1 = Lo(data_i)&0x0F;
    tmp1 = tmp1 << 6;
    tmp2 = Lo(data_i)&0xF0;
    tmp2 = tmp2 << 8;
    PORTF = Hi(data_i);
    PORTG = tmp1 | tmp2;
    PORTFSET = 0x1100; // SELECTIQ(RF8) = 1, RESETIQ(RF12) = 1
    PORTESET = 0x0200; // WRTIQ(RE9) = 1
    PORTFSET = 0x2000; // CLKIQ(RF13)= 1
    PORTECLR = 0x0200; // WRTIQ(RE9) = 0
    PORTFCLR = 0x2000; // CLKIQ(RF13)= 0

    tmp1 = Lo(data_q)&0x0F;
    tmp1 = tmp1 << 6;
    tmp2 = Lo(data_q)&0xF0;
    tmp2 = tmp2 << 8;
    PORTF = Hi(data_q); //Also clears RF8 and RF12
    PORTG = tmp1 | tmp2;
    PORTFCLR = 0x1100; // SELECTIQ(RF8) = 0, RESETIQ(RF12) = 0  (redundant)
    PORTESET = 0x0200; // WRTIQ(RE9) = 1
    PORTFSET = 0x2000; // CLKIQ(RF13)= 1
    PORTECLR = 0x0200; // WRTIQ(RE9) = 0
    PORTFCLR = 0x2000; // CLKIQ(RF13)= 0
   /*****************************************************/

    return;
   }
```